

648-M7

648FX-M7

661FX/GX-M7

Rev: 1.1


Revision History :


1. Ver A: Initial for 661FX/648FX for LGA775
2. Ver 1.0:
 - I. modify CPU pull-high
 - II. add FSB1066 select CKTs
 - III. modify Common-Choke and R0603 co-lay
 - IV. add 1394A3 header
 - V. AD1888 and ALC655 co-lay
 - VI. modify FAN CTRL CKTs
 - VII. modify VRDGD
 - VIII. add PANEL2
3. Ver 1.1:
 - I. modify for EE CPU supporting
 - II. modify SmartFAN clamp up circuit

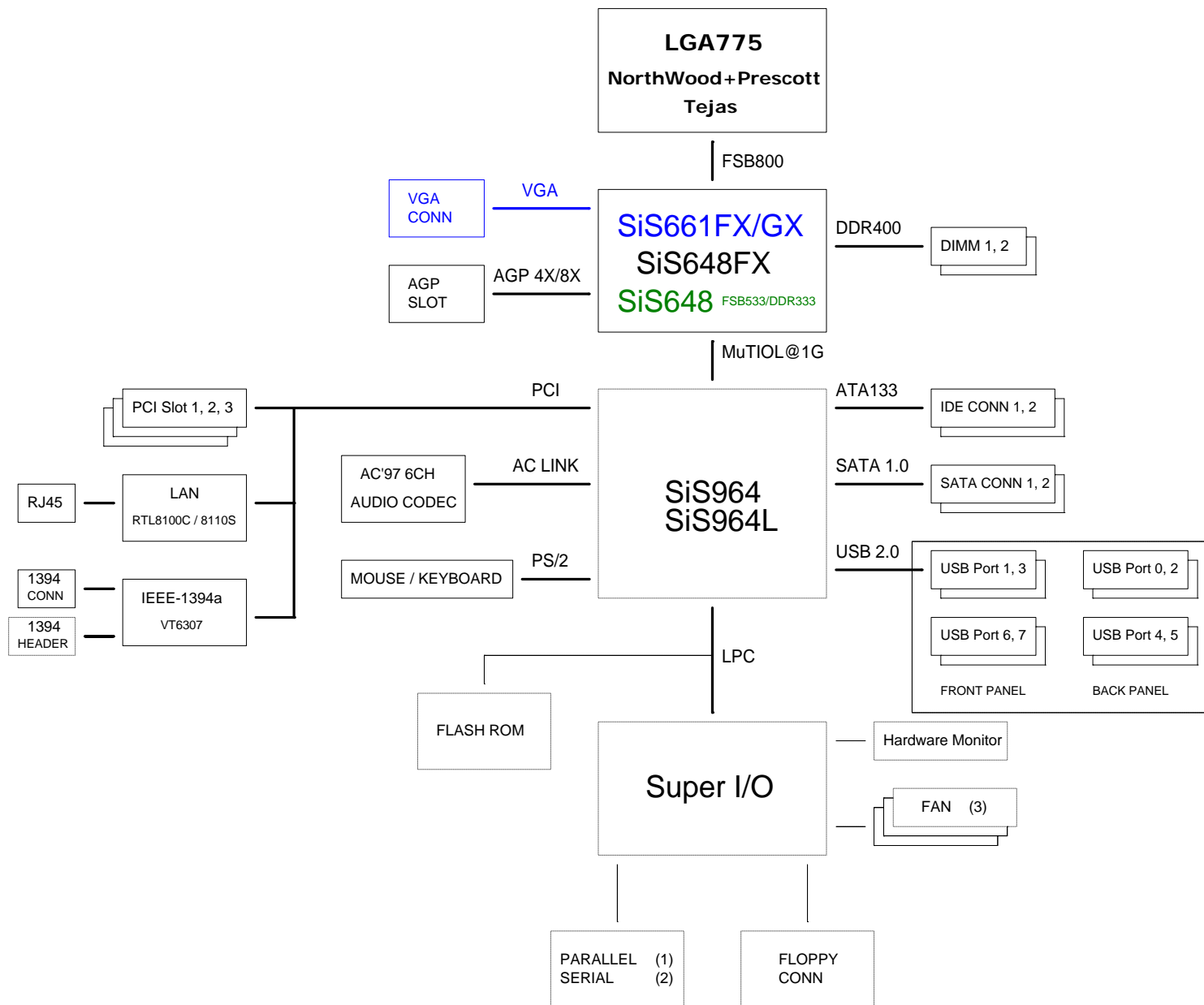
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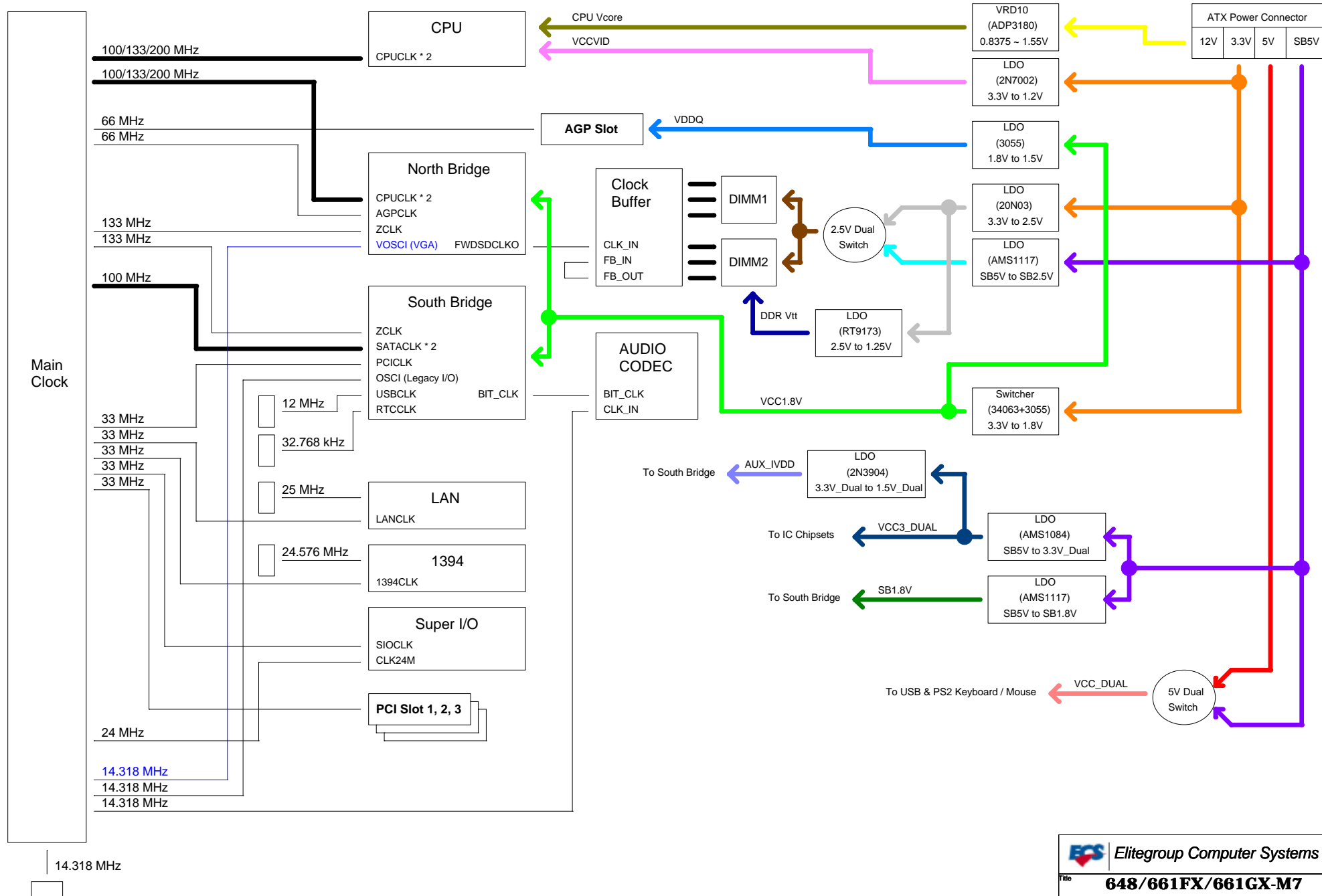
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|-------------------------------------|-------------------------------|
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| 5. Socket LGA775-2 | 25. IEEE1394a |
| 6. Socket LGA775-3 | 26. Audio Codec |
| 7. SiS661FX-1 (HOST / AGP) | 27. Audio Interface |
| 8. SiS661FX-2 (Memory) | 28. Super I/O |
| 9. SiS661FX-3 (VGA / HyperZip) | 29. KB/MS/ROM/FDC/IR |
| 10. SiS661FX-4 (Power) | 30. COM 1,2 / LPT |
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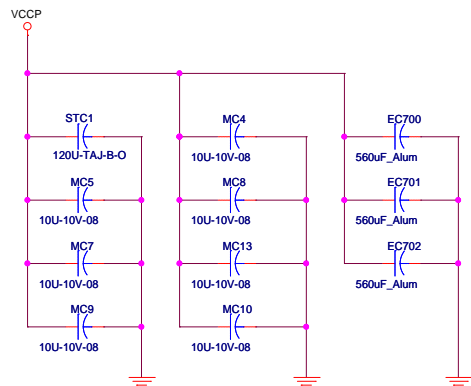
	SIGNATURE	DATE
DESIGNER	Prowind	
LAYOUT	ECS Layout team	
CHECK	Prowind Chiang	
APPROVAL		

	Elitegroup Computer Systems		
Title	648/661FX/661GX-M7		
Size	Document Number	Cover Sheet	Rev 1.1
Date	Monday, March 14, 2005	Sheet 1 of 36	

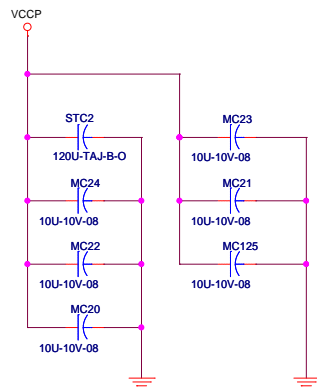




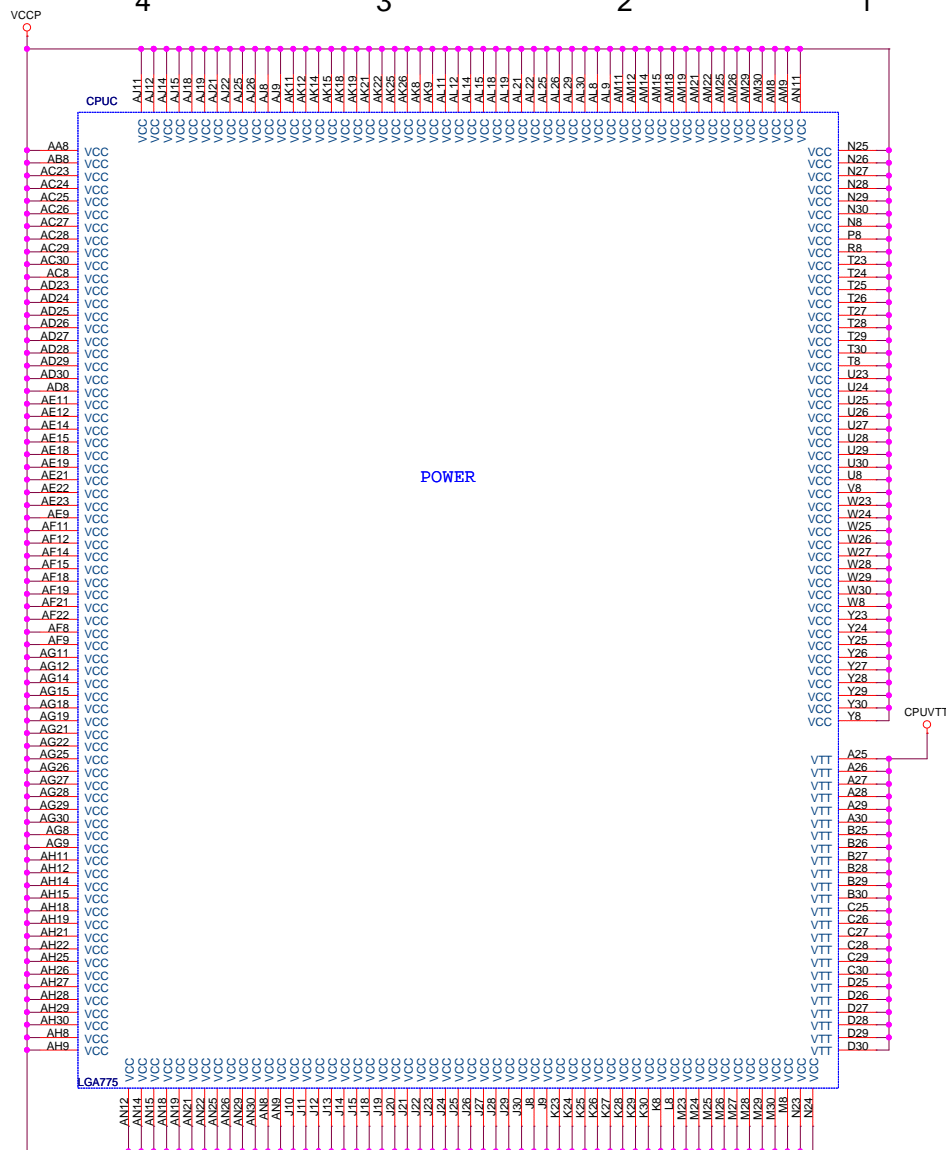
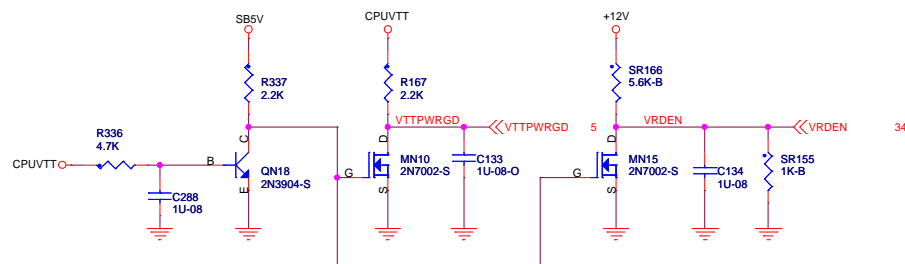
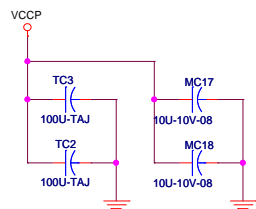
Put these capacitors at processor TOP SIDE



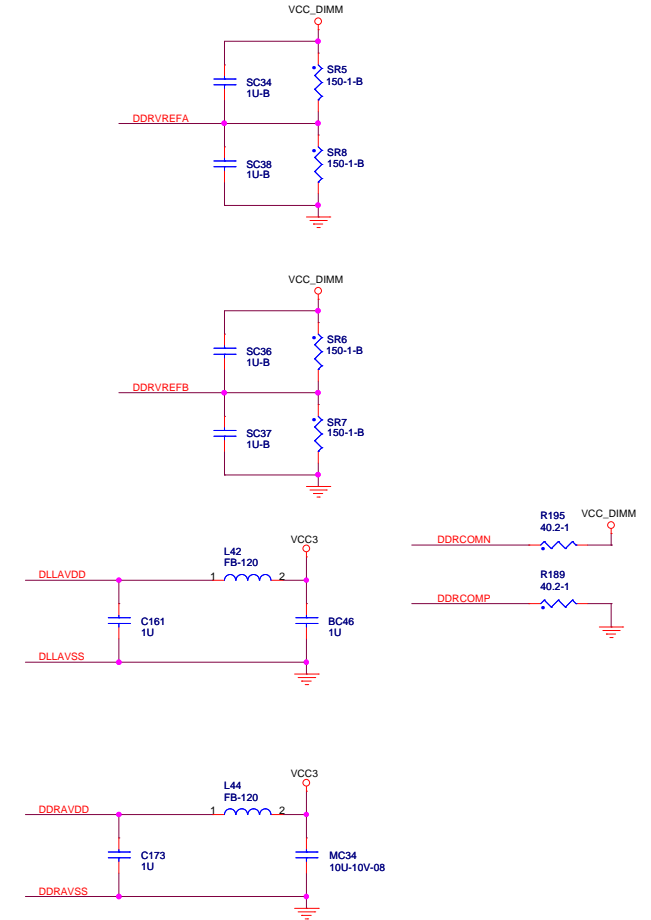
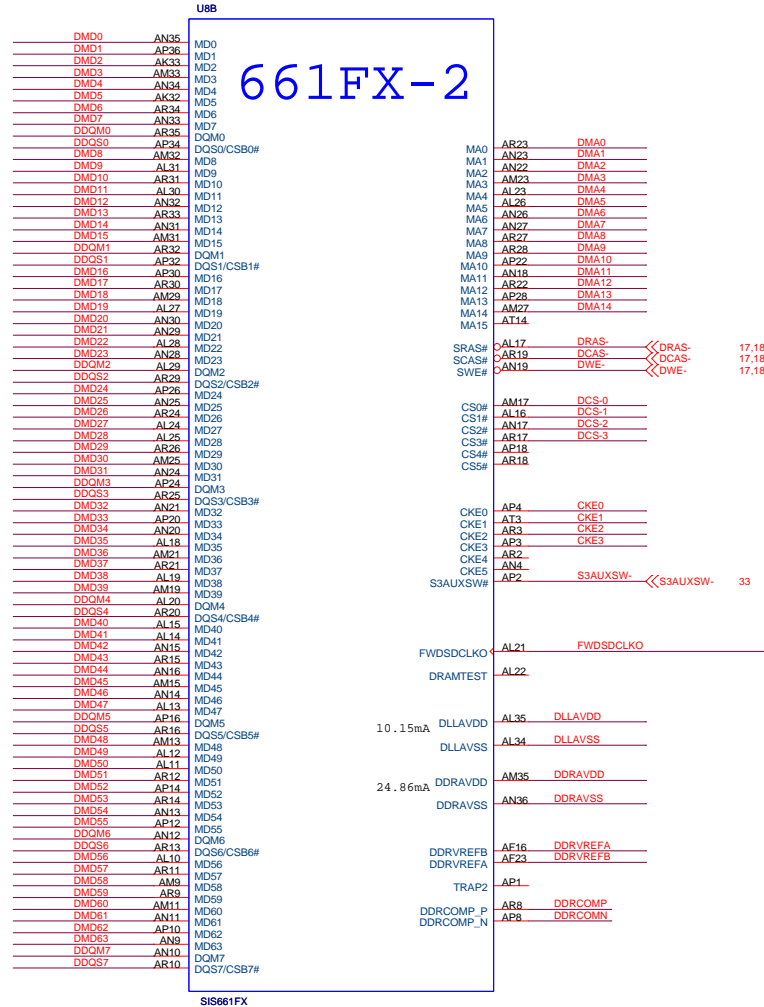
Put these capacitors at processor LEFT SIDE



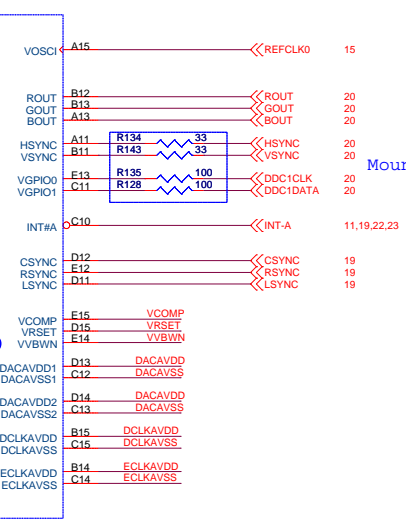
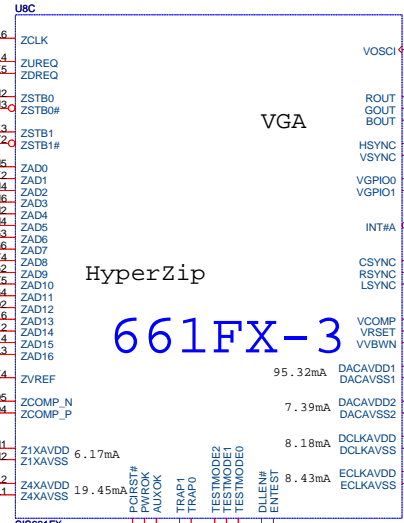
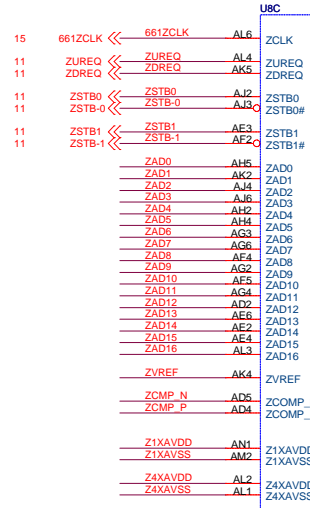
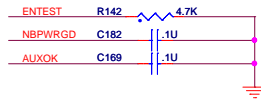
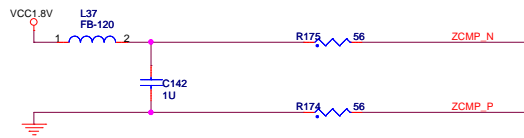
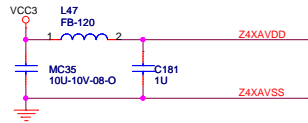
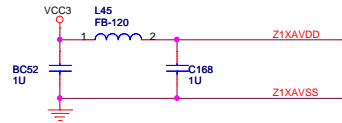
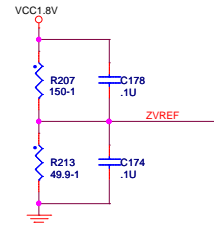
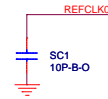
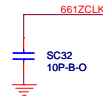
Put these capacitors INSIDE PROCESSOR CAVITY



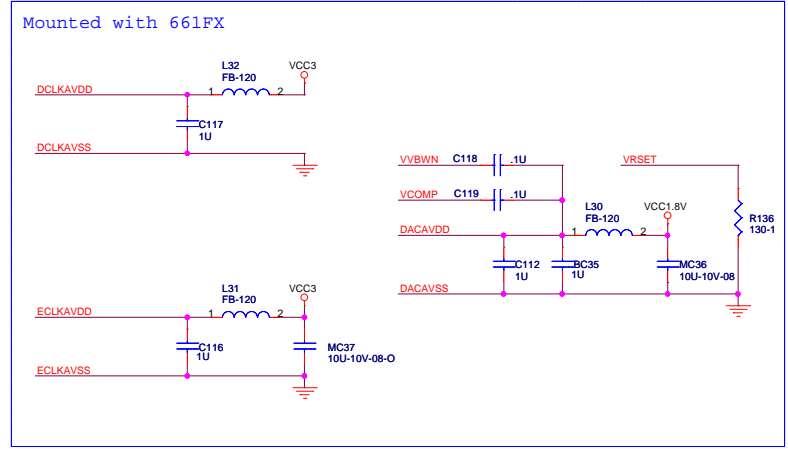
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DDQM[0..7] <<DDQM[0..7] 17,18
DDQS[0..7] <<DDQS[0..7] 17,18
DMA[0..14] <<DMA[0..14] 17,18
DCS-[0..3] <<DCS-[0..3] 17,18
CKE[0..3] <<CKE[0..3] 17



11 ZAD[0..16] << ZAD[0..16]



Mounted with 661FX



661FX-4

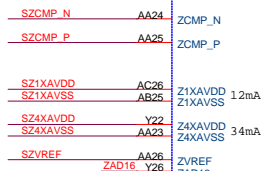
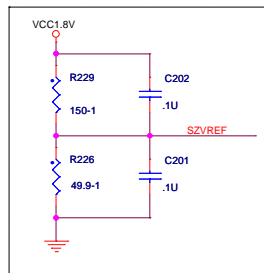
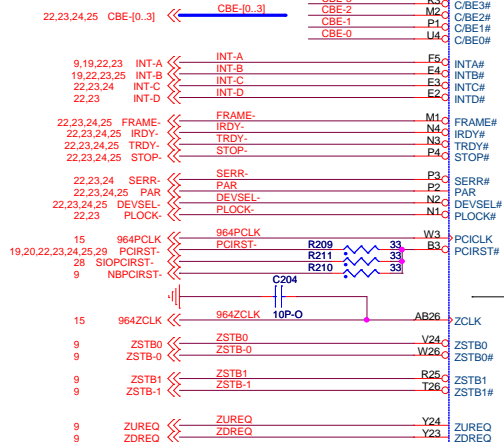
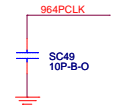
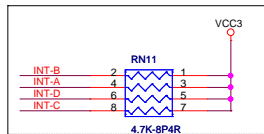
Power

NOTE:
SIS648FX doesn't have
the following 9 balls
VDDQ(P12), VDDM(AE14), VDDM(AE15),
VDDQ(AB25), IVDD(N20), IVDD(T24),
VTT(N20), VTT(N25), VTT(P25).

AUX_IVDD=10.12mA
AUX3.3=26.38mA

Place these capacitors under 648 solder side

But SIS648 and SIS660 still
have these 9 balls.

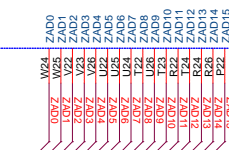


PCI

IDE

964-1

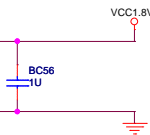
HyperZip



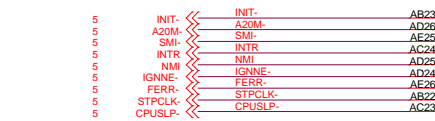
10mA

U13A

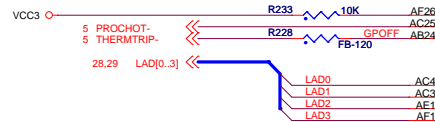
SIS964



Programable on-die pull-high strength for CPU_S:
(Infinite, 150, 110, 56 Ohm)



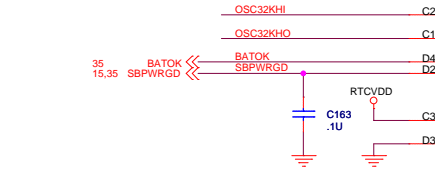
CPU_S



APIC

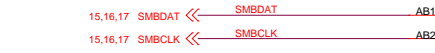


LPC

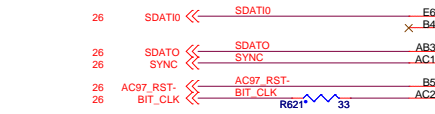


RTC

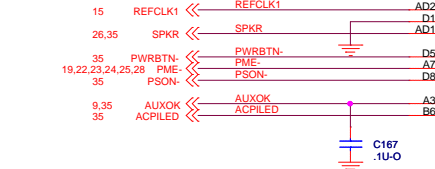
964-2



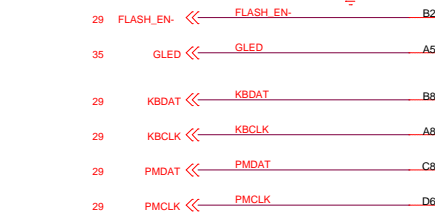
GPIO



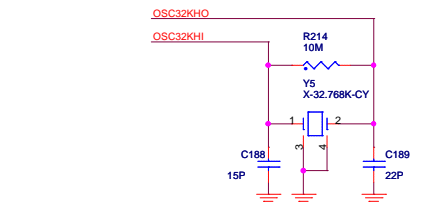
AC97



ACPI
/others

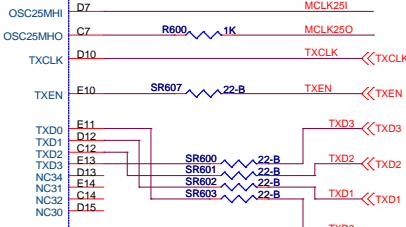


KBC
/geyserville

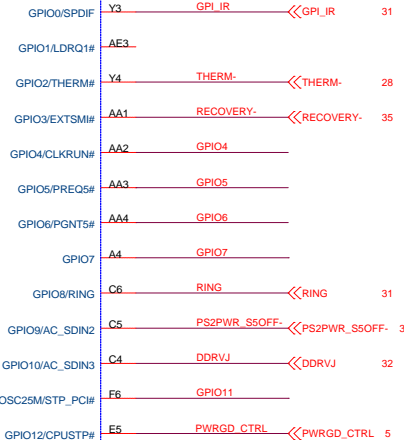


BIT_CLK

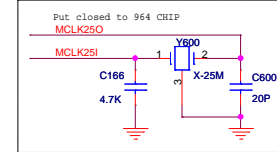
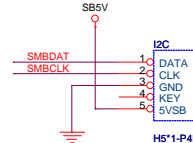
MII



1mA

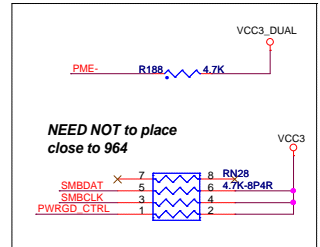
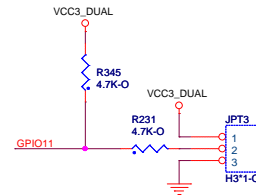
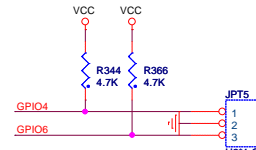
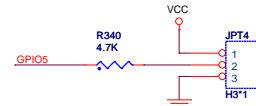


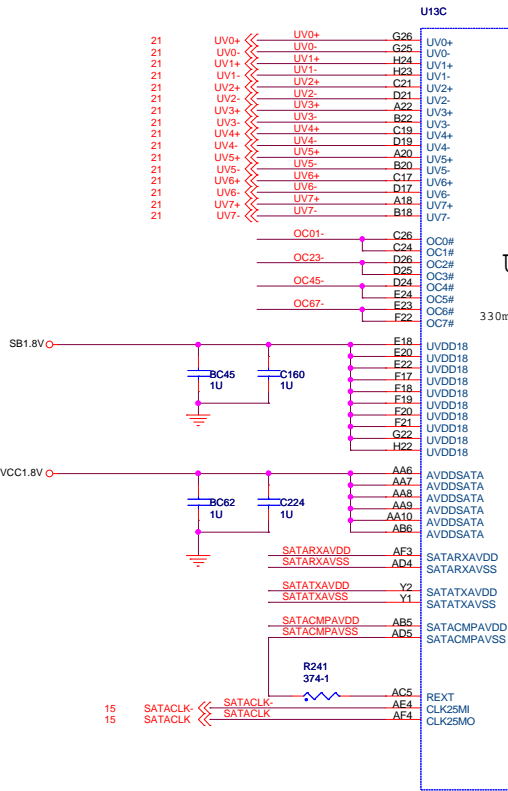
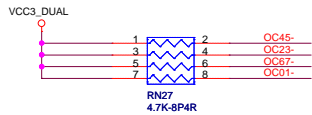
SIS964



	SB GPIO	Function	High(1-2)	Low(2-3)
JPT4	GPI5	Suspend Mode	S1 & S3	S1 only
	GPI7	LAN Select	PCILAN	LANPHY
	GPO9	S5 Wake-up	Enable	Disable
JPT3	GPI11	CPU Select	04B/FMB1.5	04A/FMB1.0
	GPI012	CPUPWRGD_CTRL	By SIS Programming Guide	
	GPO13	Flash EN-	Write Enable	Write Disable
	GPO2	ThermWarming-	Normal	OverTemp

	SIO GPIO	Function	High	Low
	GPO47	FAN_ON-	LowSpeed	HighSpeed
	GPO62	ROM_TBL-	Write Enable	Protect
	GPI66	ThermWarming-	Normal	OverTemp
	GPO67	OverTempBeep	Beep	Normal

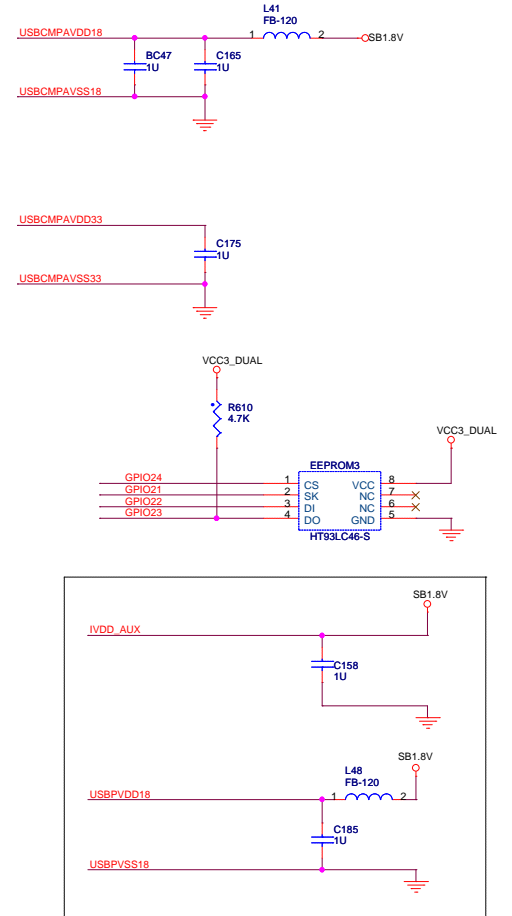
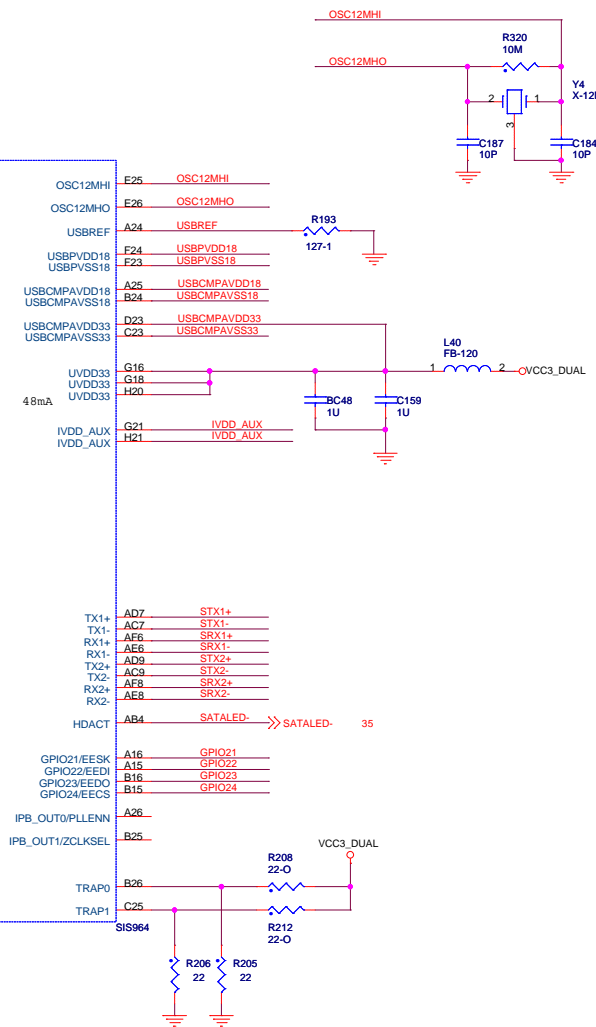
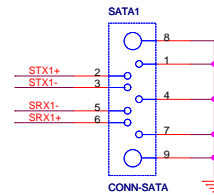
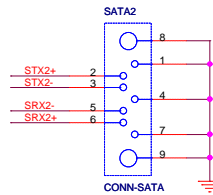
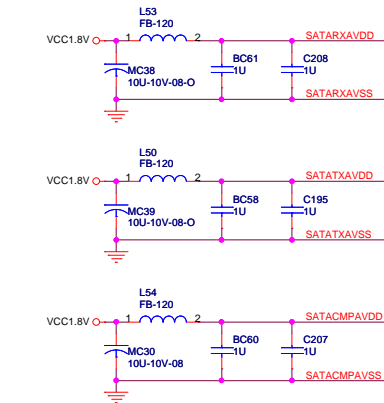


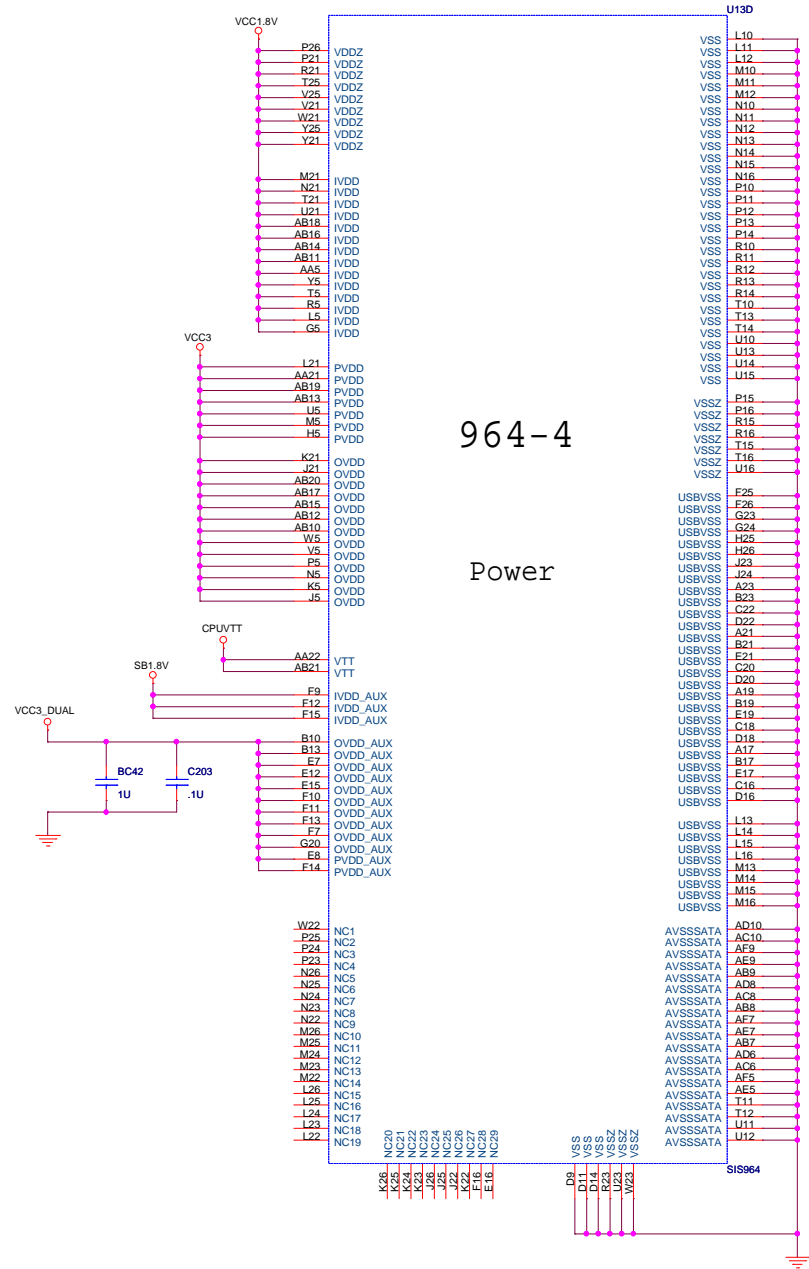
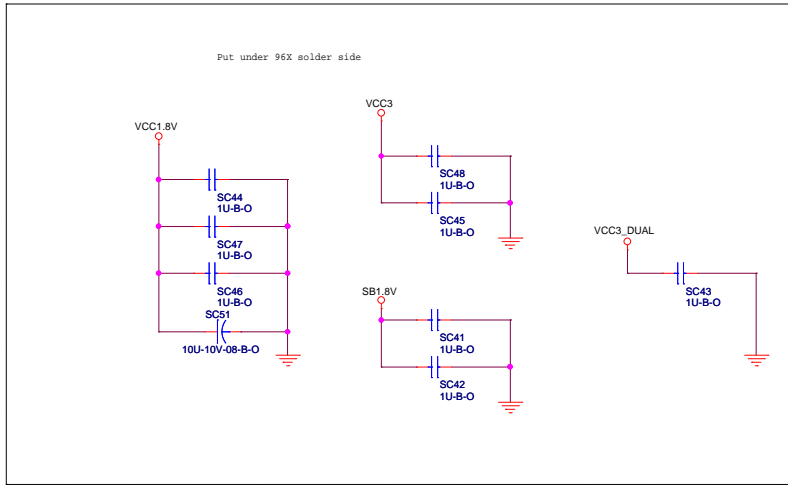
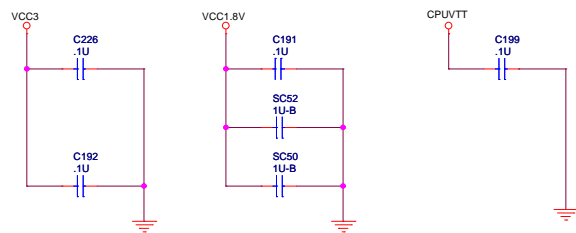


USB

964-3

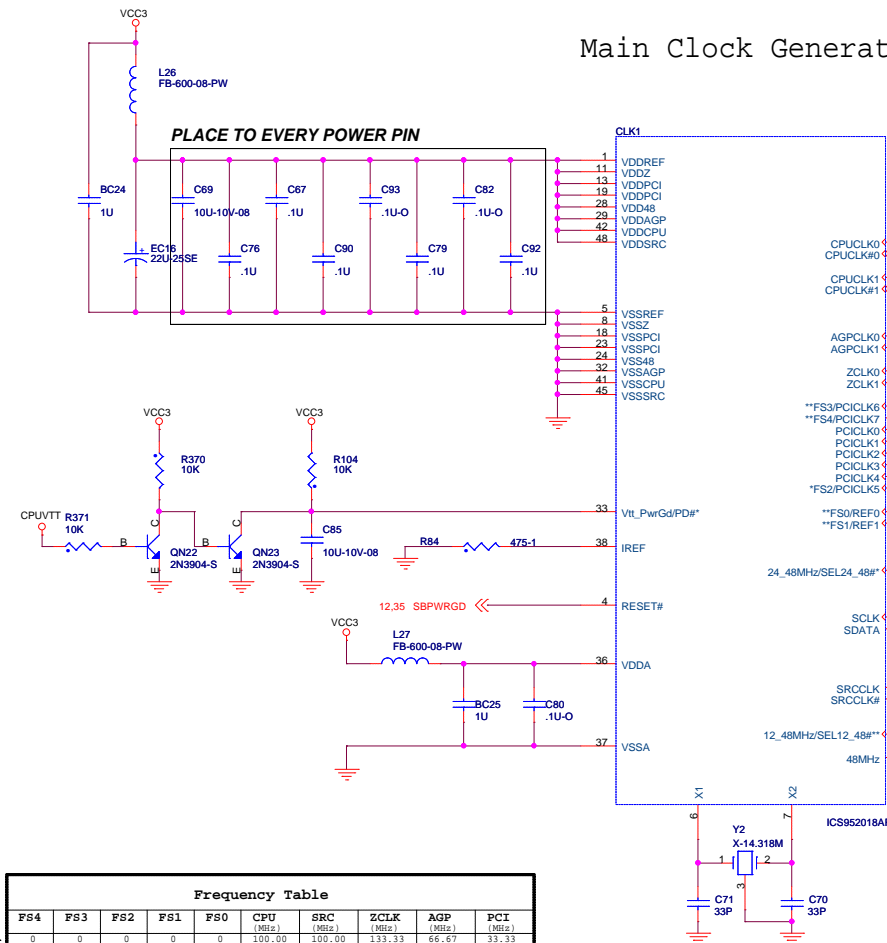
330mA



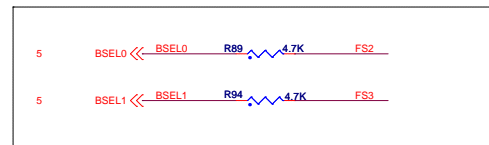


964-4
Power

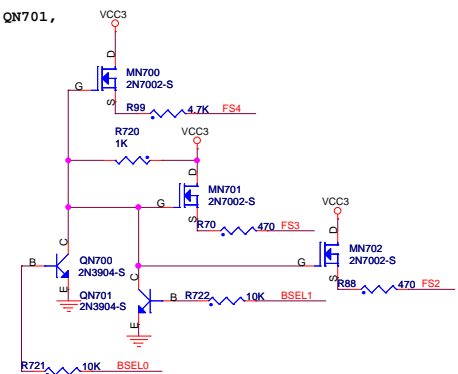
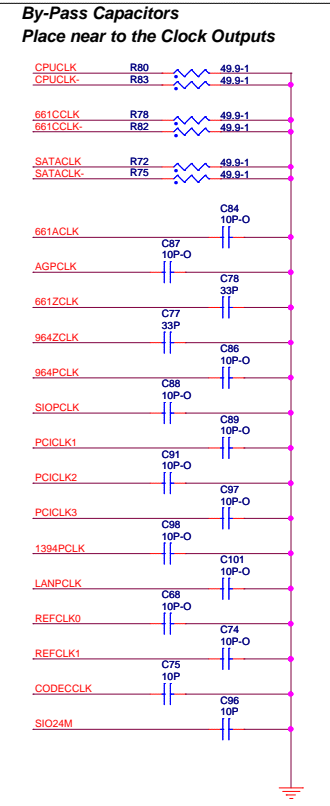
Main Clock Generator



Frequency Selection



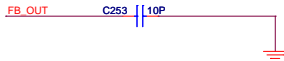
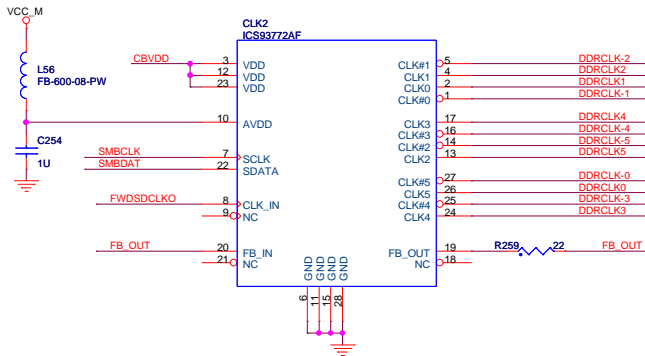
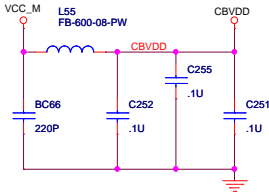
Clock Generator Table	FS4	FS3	FS2	FS1	FS0
Hardware Trapping	Low	Low	BSEL2	BSEL1	BSEL0
CPU=100 (BSEL[2:0]=101)					
CPU=133 (BSEL[2:0]=001)	0	0	1	0	0
CPU=166 (BSEL[2:0]=011)	0	1	1	0	0
CPU=200 (BSEL[2:0]=010)	0	1	0	0	0
CPU=266 (BSEL[2:0]=000)	1	1	1	0	0



Clock Buffer (DDR)

{5 OPTIONS}
1: (ICS) ICS93716
2: (Winbond)
3: (ICWorks)
4: (IMI)
5: (AMI)

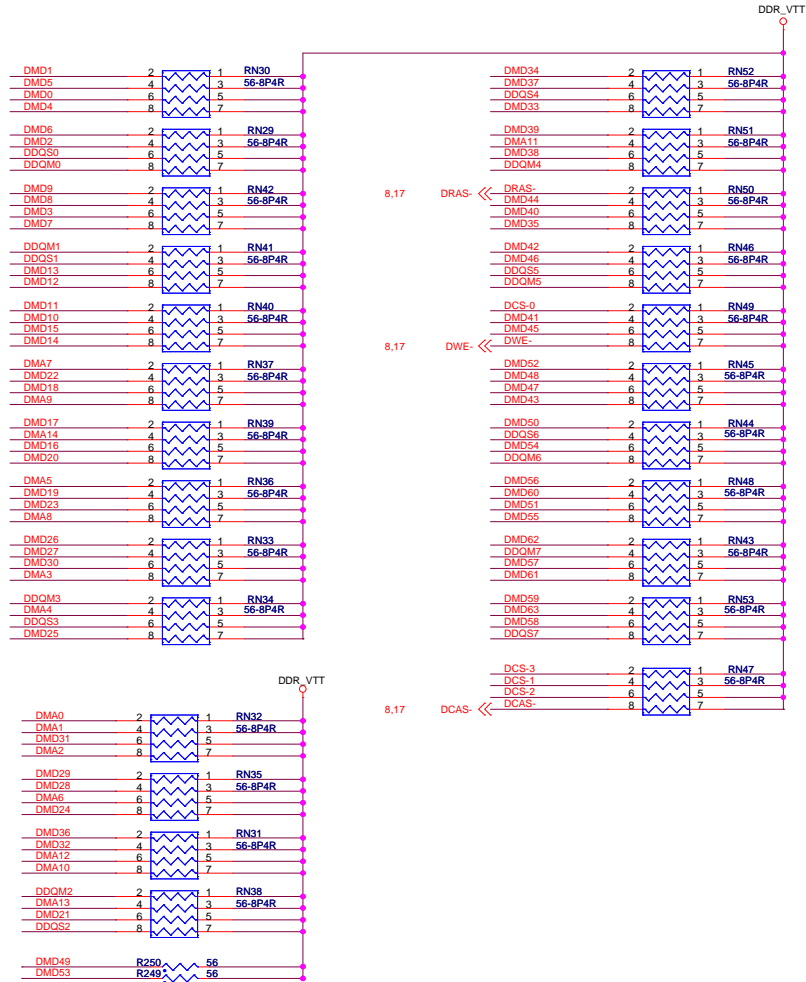
By-Pass Capacitors
Place near to the Clock Buffer



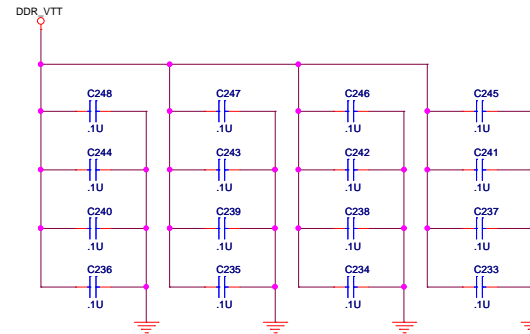
SSTL-2 Termination Resistors

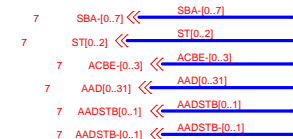
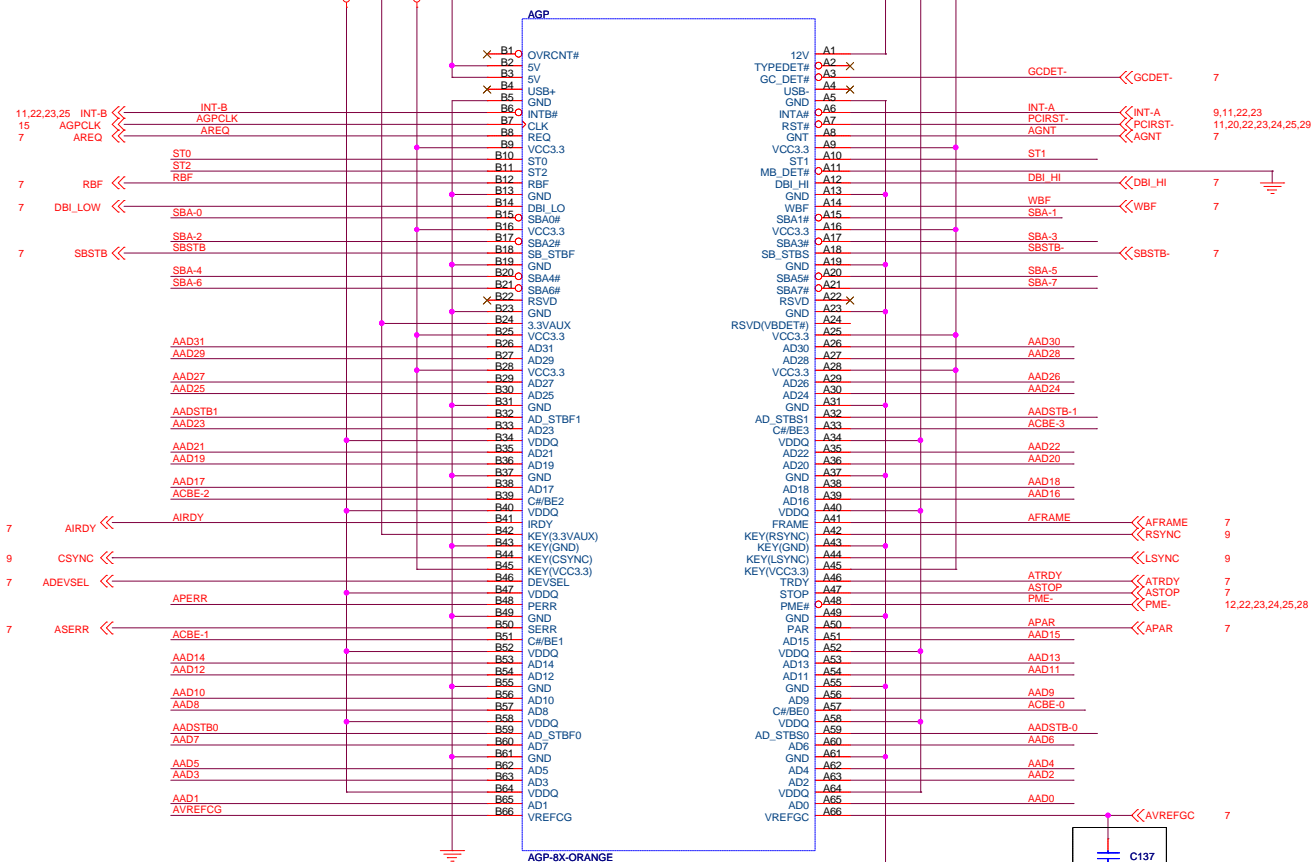
	SDR		JDR		
VD/DQM(/DQS)	LV-CMOS	Ra	0/10/-	Ra	0
MA/Control	LV-CMOS		SSTL-2		0
CS	LV-CMOS		SSTL-2		0
WE	DD 3.3V		DD 2.5V		0

DMD[0..63]	<<DMD[0..63]	8,17
DMA[0..14]	<<DMA[0..14]	8,17
DDQM[0..7]	<<DDQM[0..7]	8,17
DDQS[0..7]	<<DDQS[0..7]	8,17
DCS[0..3]	<<DCS[0..3]	8,17

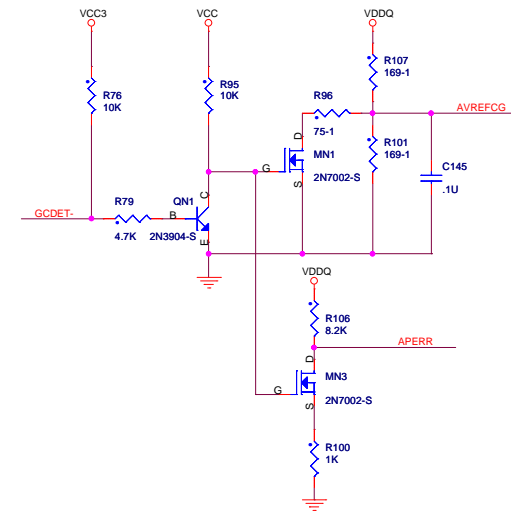


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
 0603 Package placed within 200mils of VTT Termination R-packs



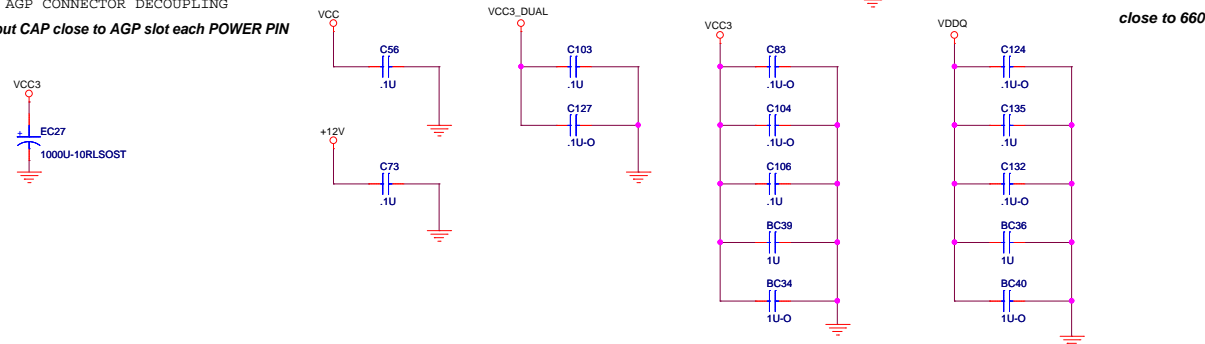


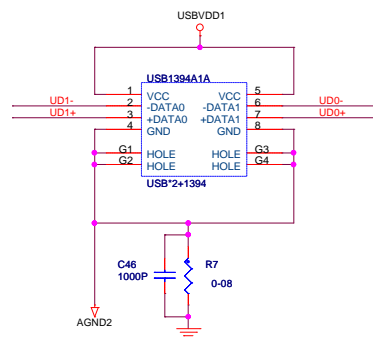
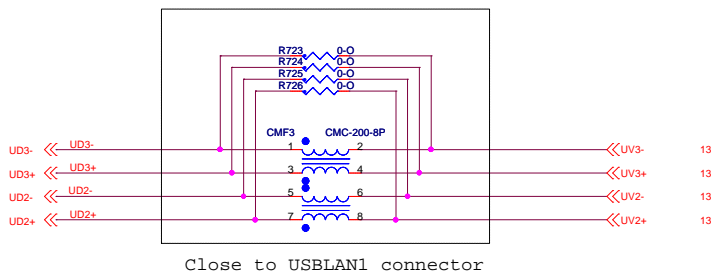
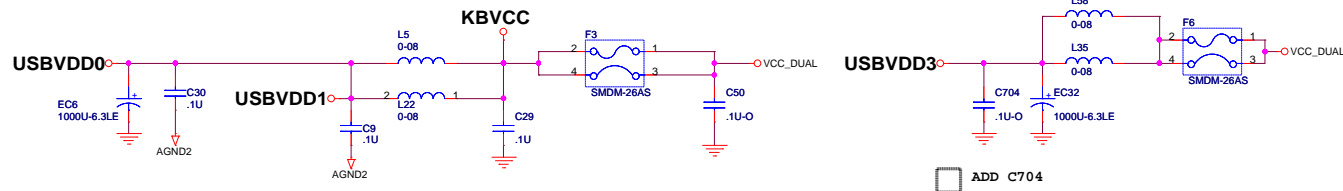
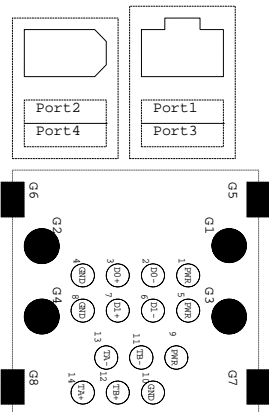
GCDET-	Low	Hi
Graphic Card	AGP 3.0	AGP 2.0
AVREFCG	0.35	0.75
APERR	0	1.5



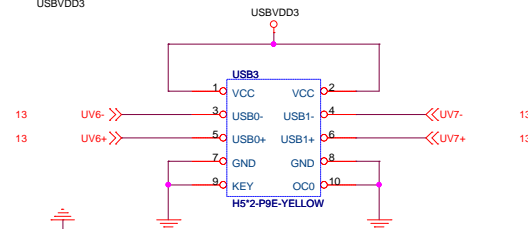
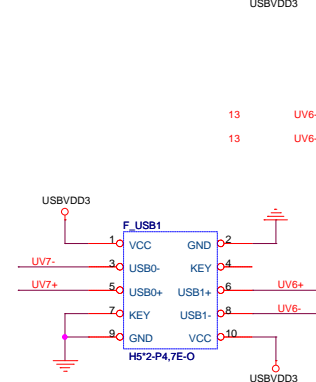
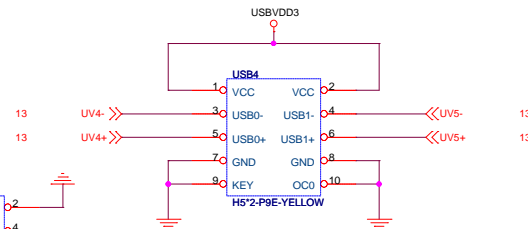
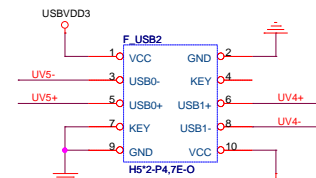
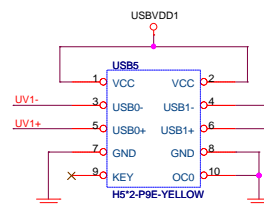
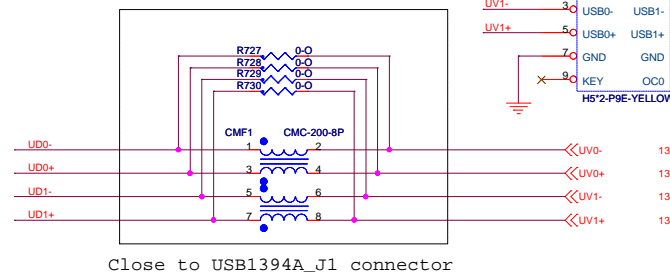
AGP CONNECTOR DECOUPLING

put CAP close to AGP slot each POWER PIN

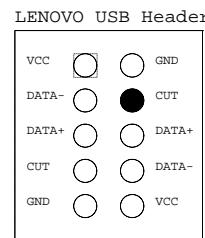
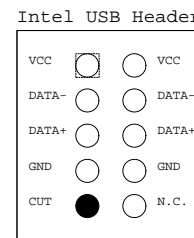
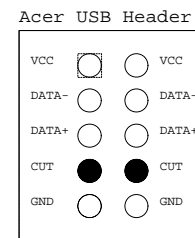
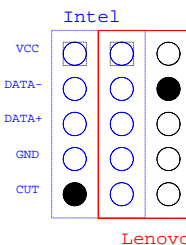
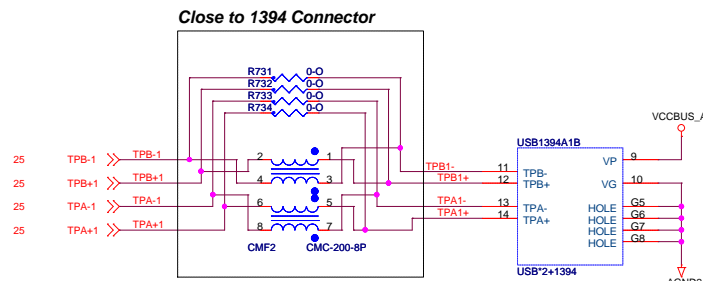
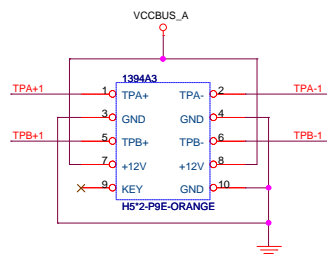




	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5

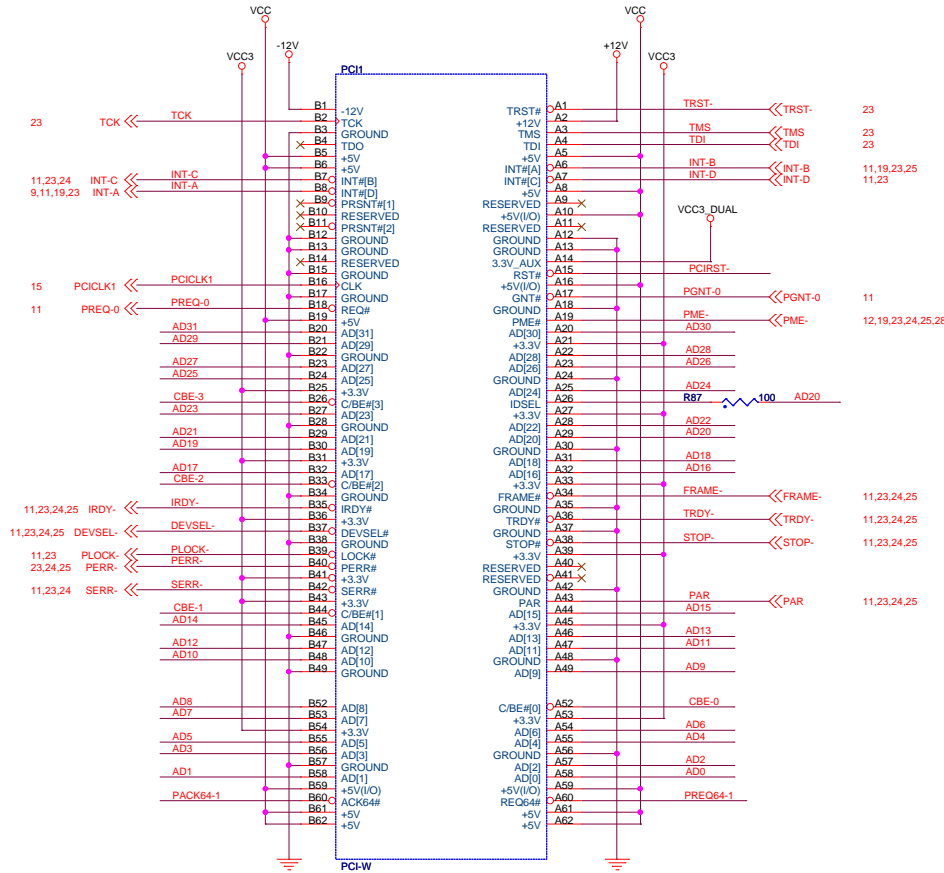


ADD 1394A3

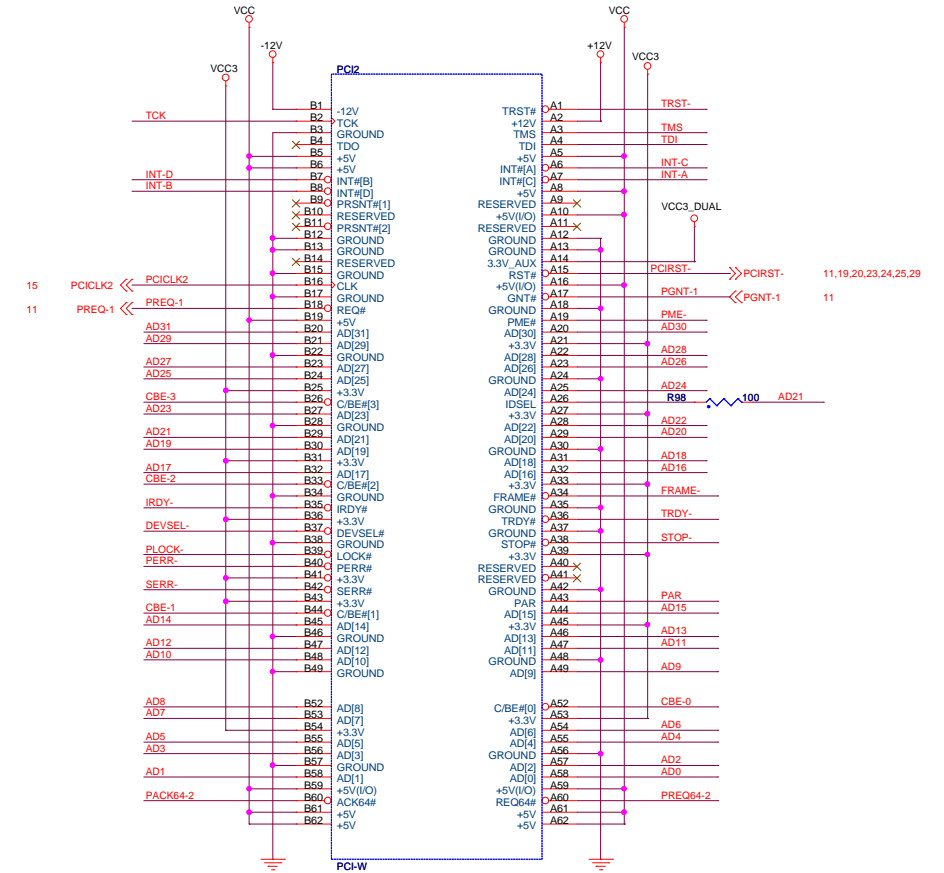


PCI Slot 1 & 2

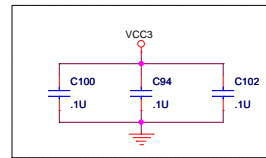
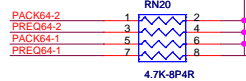
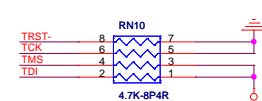
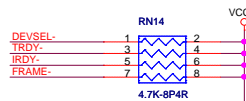
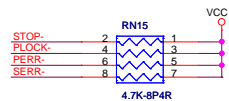
11,23,24,25 CBE[0..3] << CBE[0..3]
11,23,24,25 AD[0..31] << AD[0..31]



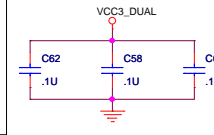
IDSEL=AD20
INT[B,C,D,A]

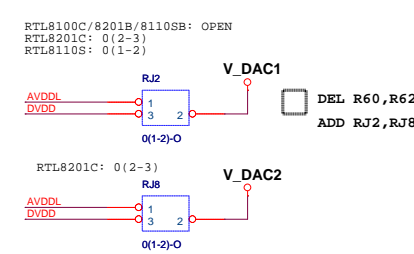
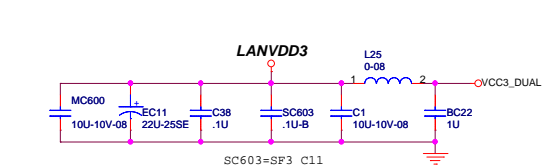


IDSEL=AD21
INT[C,D,A,B]

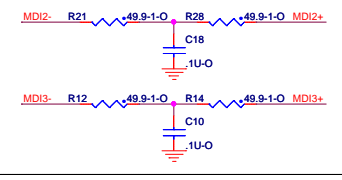


每個 PCI 插槽 pin A33
各放一顆

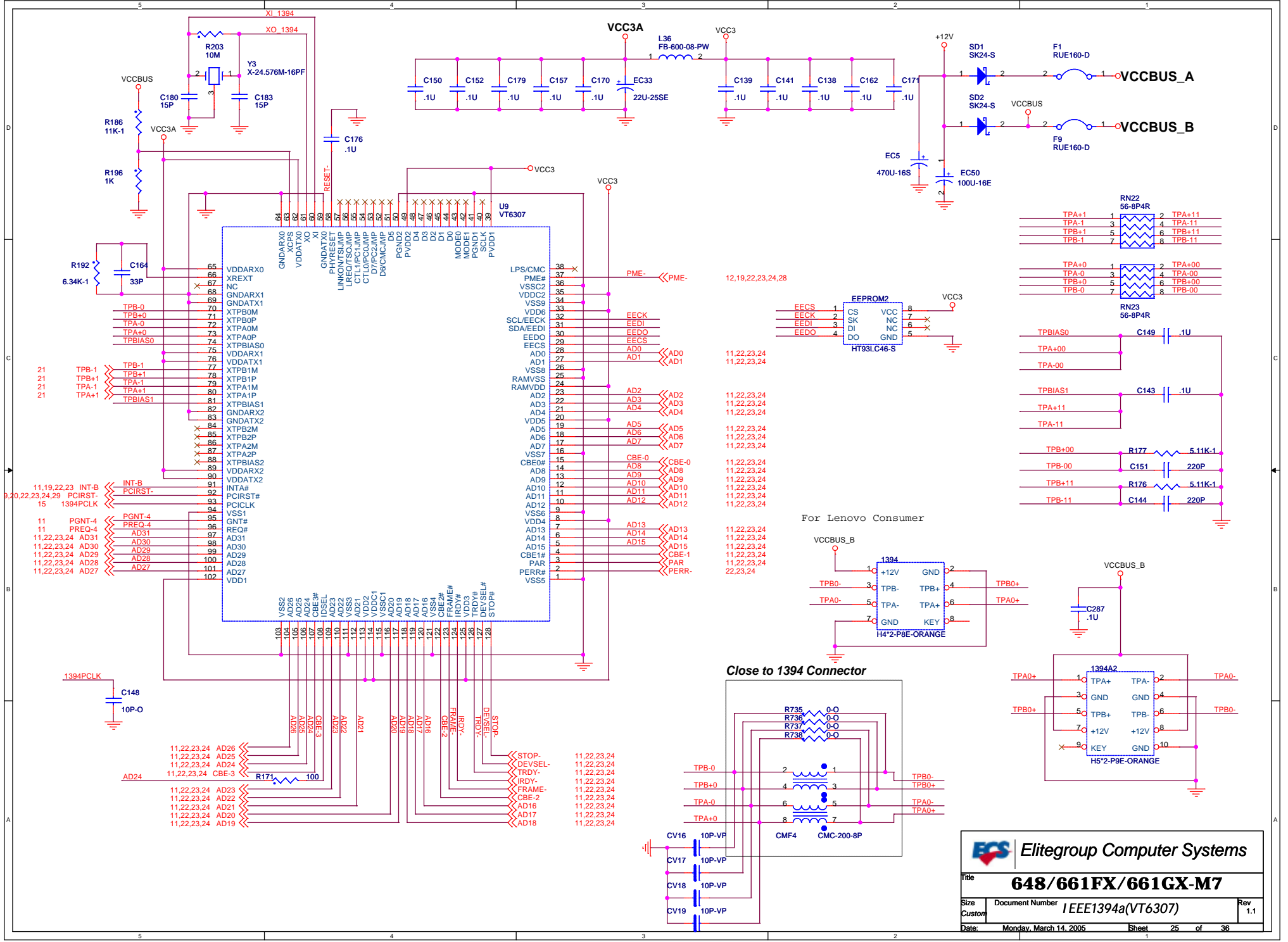


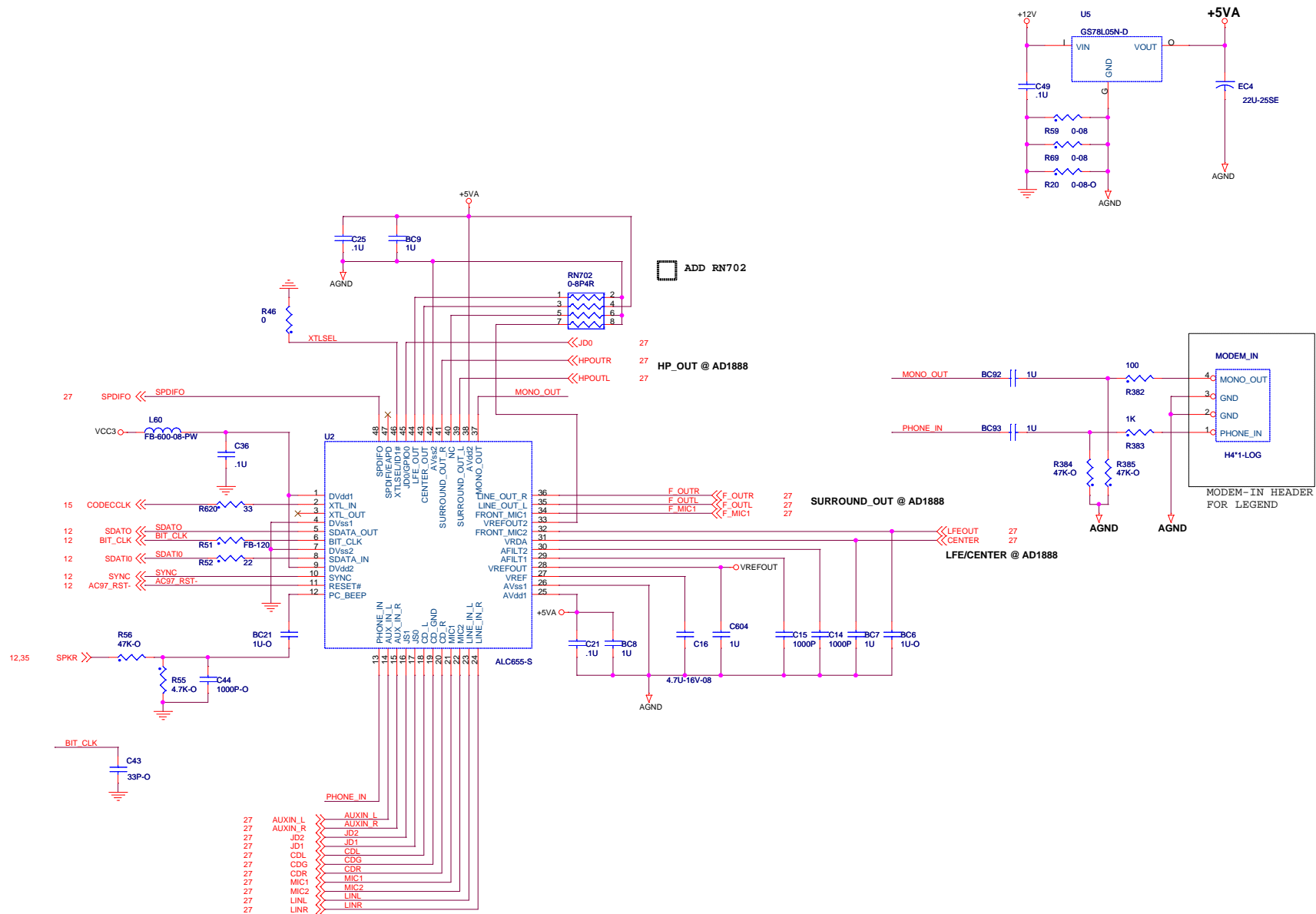
[illegible]

At RTL8100C application, use Pulse H1267.
At RTL8110S-32application use Pulse H5007.

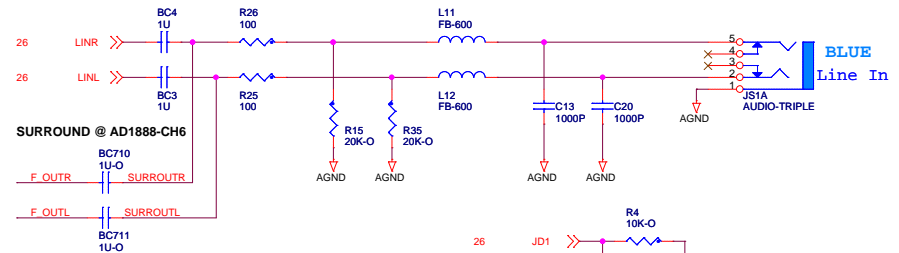
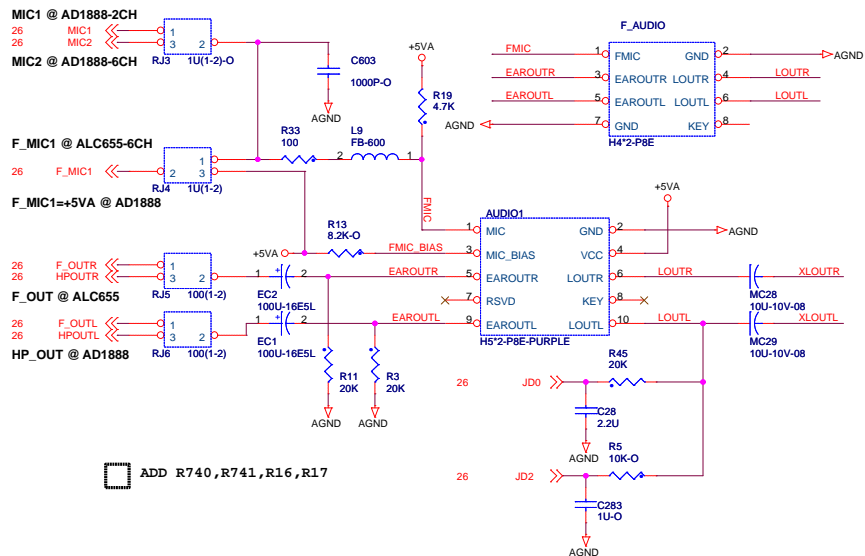


```
RTL8100C: OPEN
RTL8110S: Mounted
```

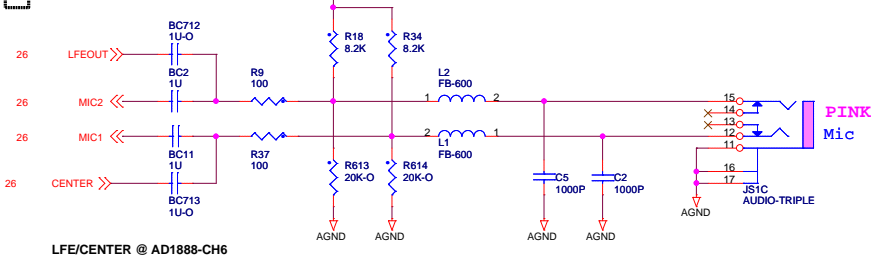


ADD BC708, BC709, R739, BC1



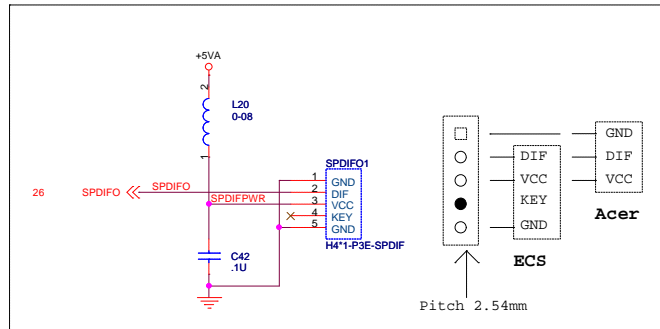
ADD BC710, BC711

ADD BC712, BC713

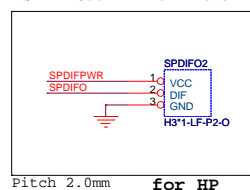


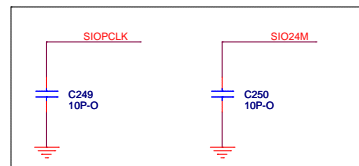
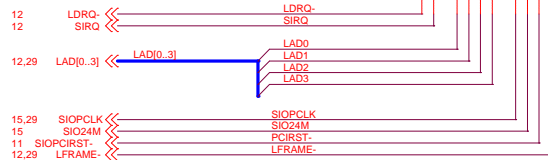
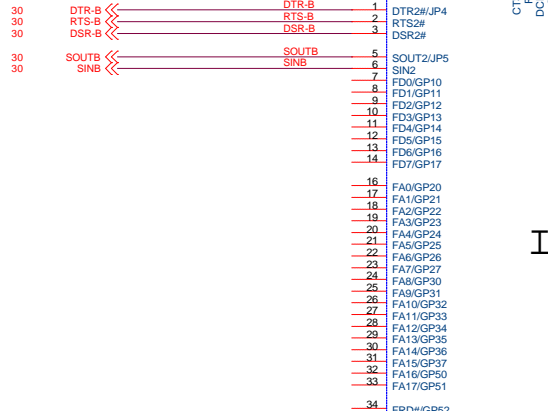
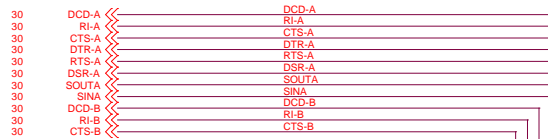
ADD ACER 3-PIN SPEC

SPDIF-Out Pin Definition1



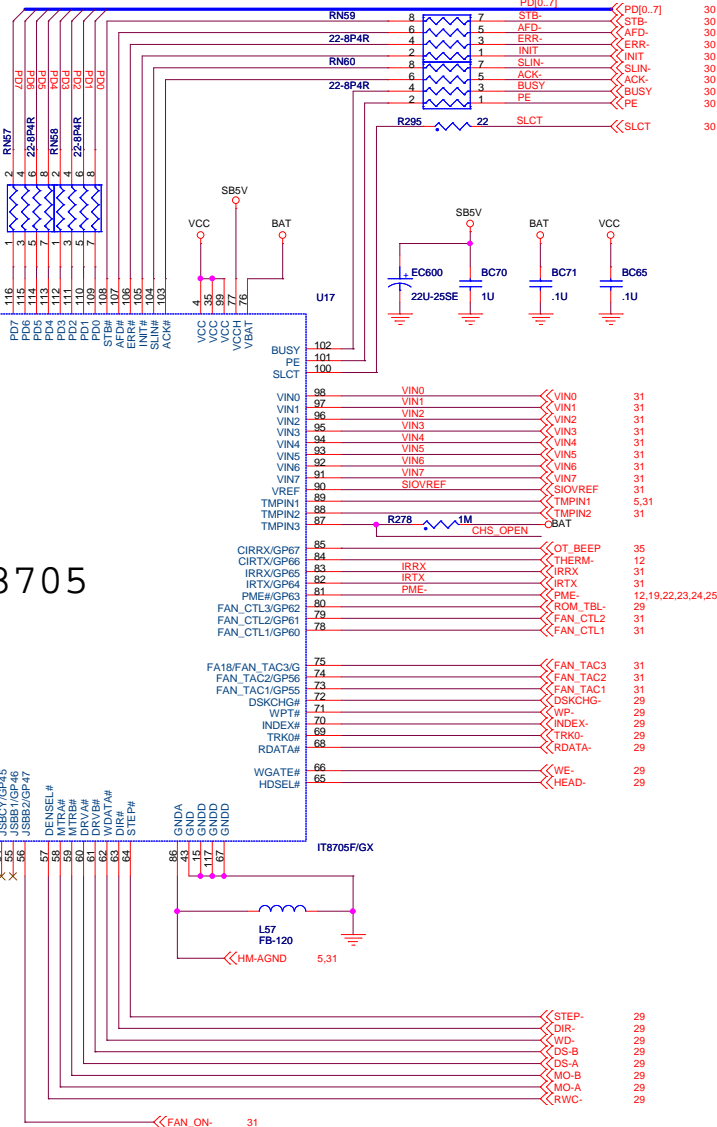
SPDIF-Out Pin Definition2



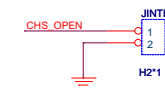


Place near to ITE8705

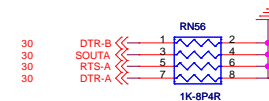
ITE 8705



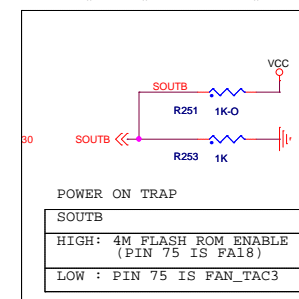
		High	Low
GPIO62	BootBlockProtect	Disable	Enable



ITE 8705 POWER ON TRAPS

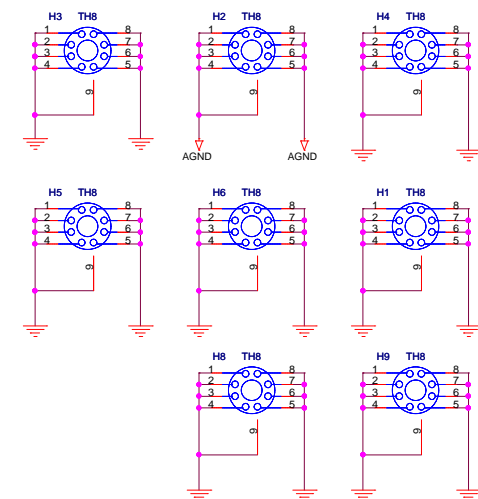
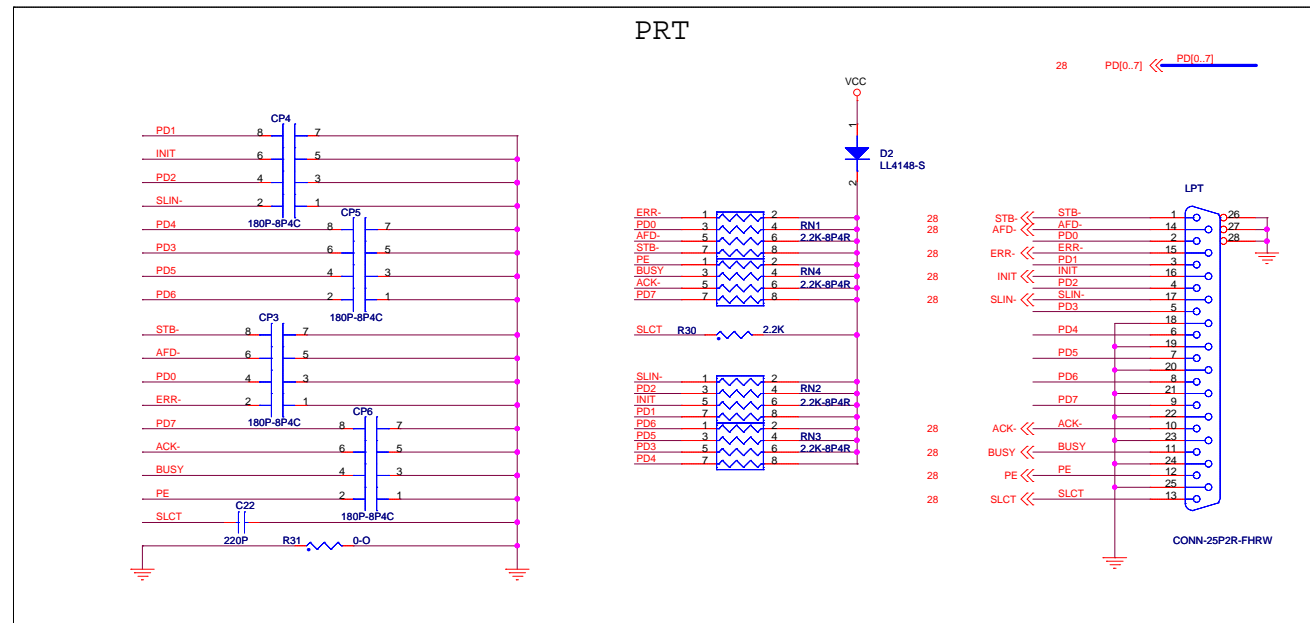
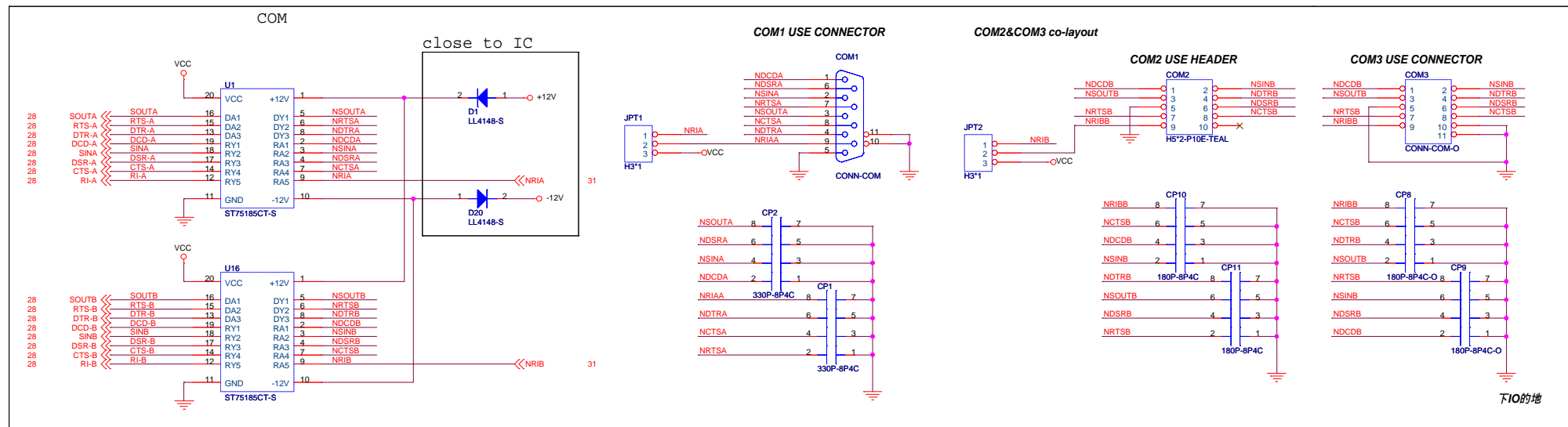


- 1.If use LPC ROM, pull down DTR#A RTS#A SOUTA DTR#B
- 2.If use Legacy 2MB flash rom, pull high DTR#A RTS#A SOUTA DTR#B
- 3.If use Legacy 4MB flash rom, pull high DTR#A RTS#A SOUTA DTR#B

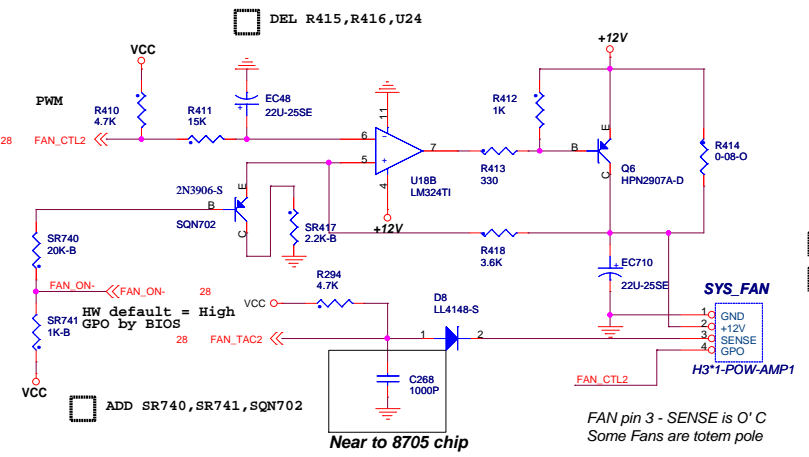
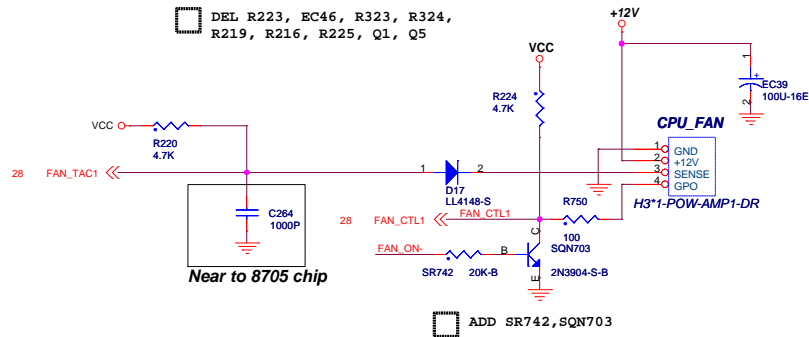


POWER ON TRAP

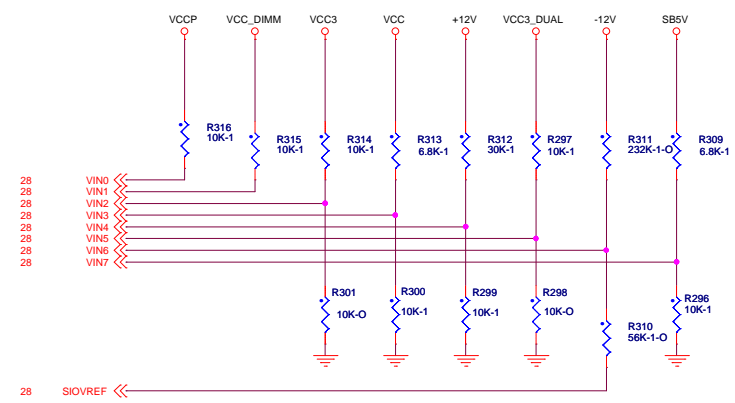
SOUTB
HIGH: 4M FLASH ROM ENABLE (PIN 75 IS FA18)
LOW : PIN 75 IS FAN_TAC3



Layout :
Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

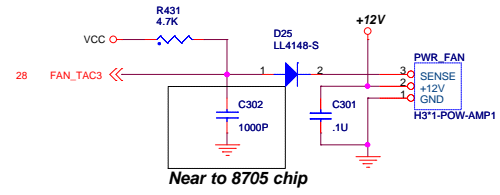


Voltage Monitor



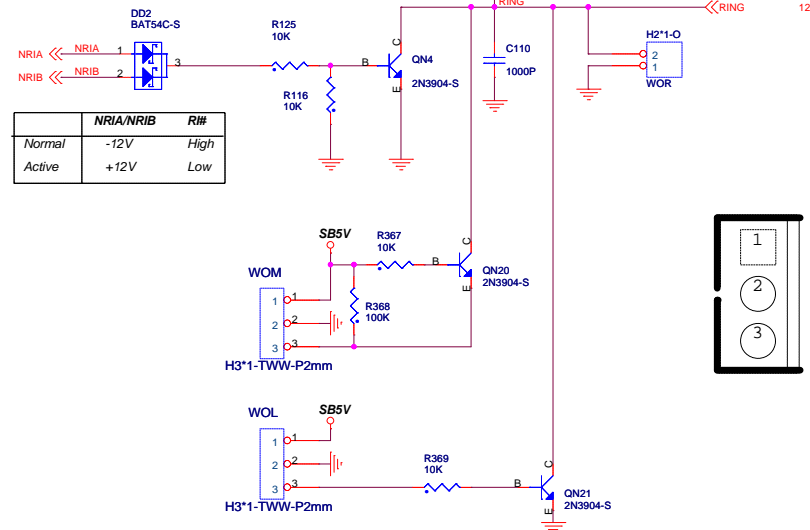
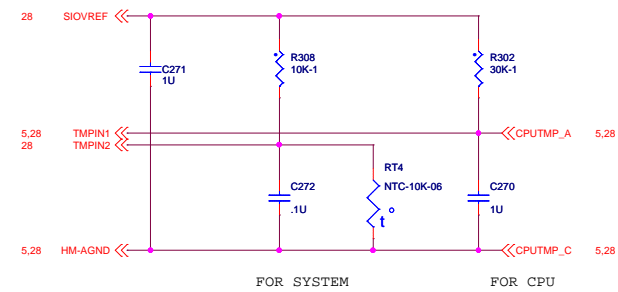
FAN pin 3 - SENSE is O' C
Some Fans are totem pole

- DEL D700
- modify SQN702, SR740, SR741, SR742, R417-->SR417



Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode

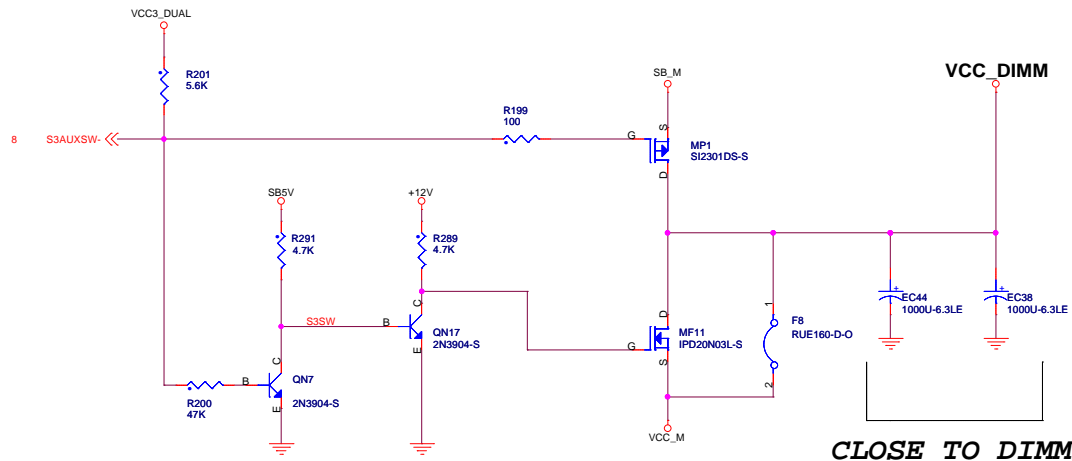
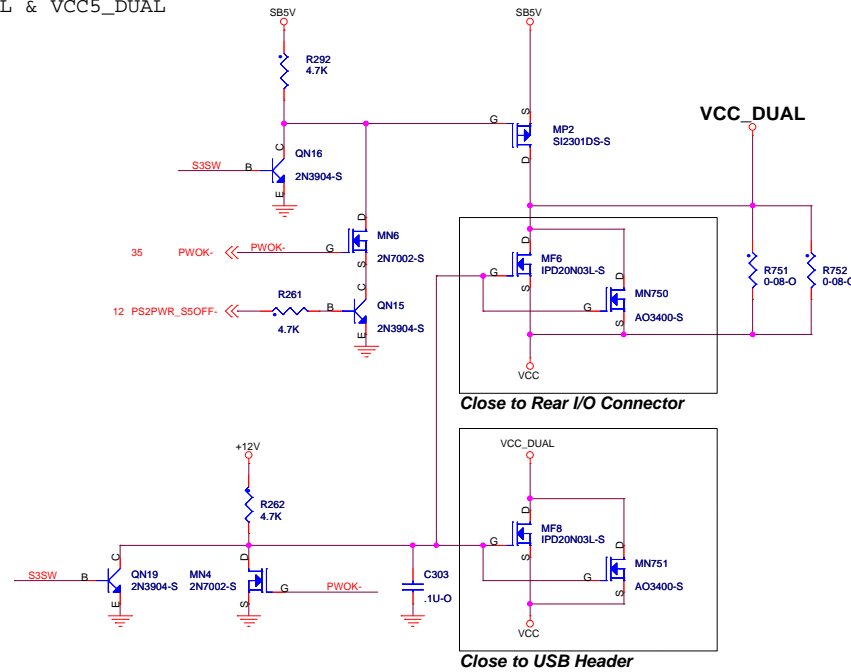



```
1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER
```

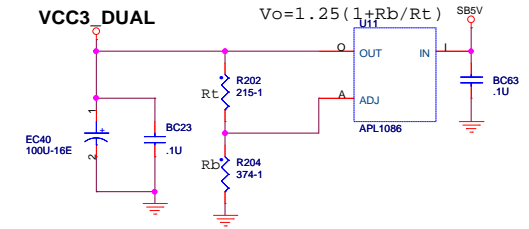
2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER. (ADDITIONAL
500mA PER USB PORT)

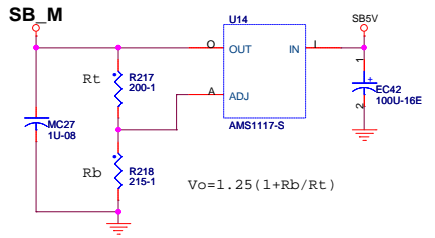
VCC3_DUAL & VCC5_DUAL



VCC3_DUAL

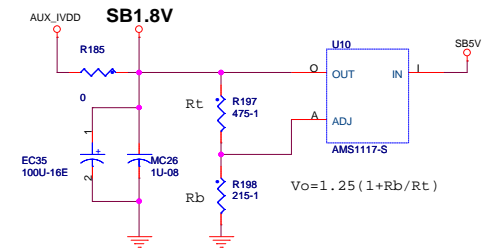


SB_M



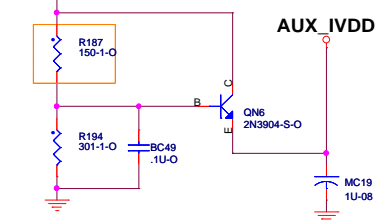
SB1.8V (For SB) 450mA

SB1.8V

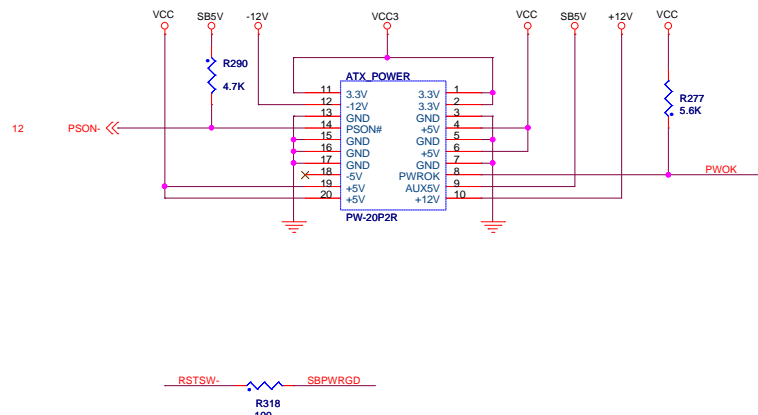


VCC3_DUAL

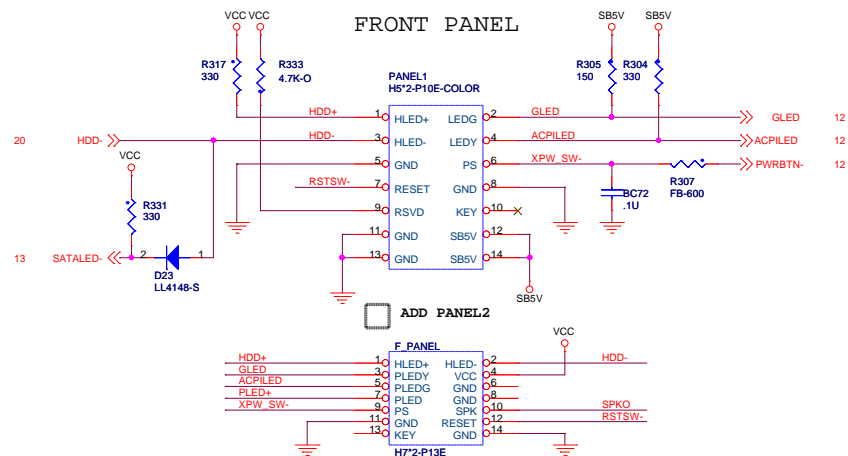
AUX_IVDD (1.5V For NB) 10mA

 Elitegroup Computer Systems

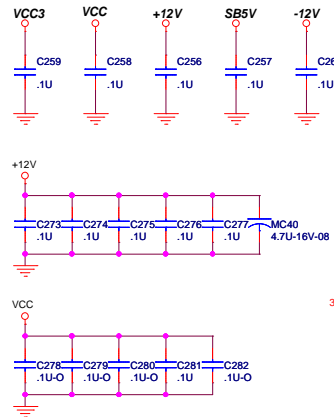
Title			
648/661FX/661GX-M7			
Size	Document Number		Rev
Custom	<i>Dual 5V&3V, STR</i>		1.1
Date:	Monday, March 14, 2005	Sheet	33 of 36



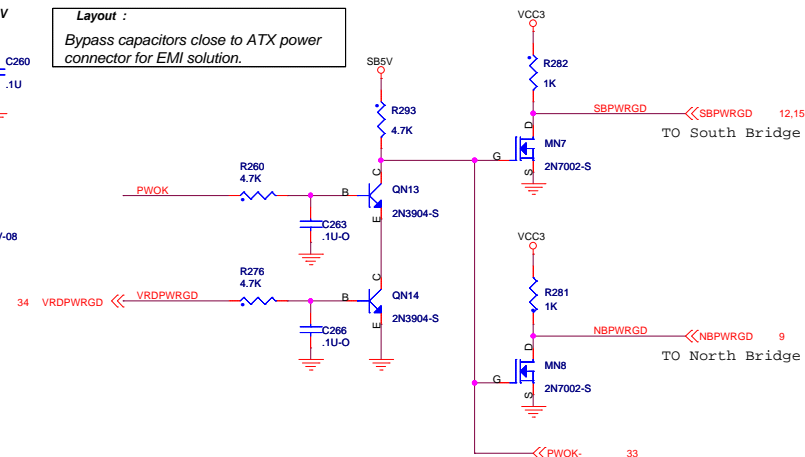
Hardware Reset Circuit



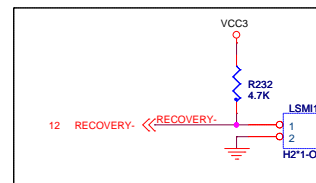
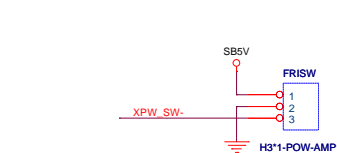
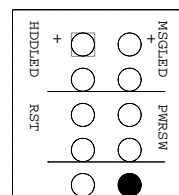
FRONT PANEL



Layout :
Bypass capacitors close to ATX power connector for EMI solution.

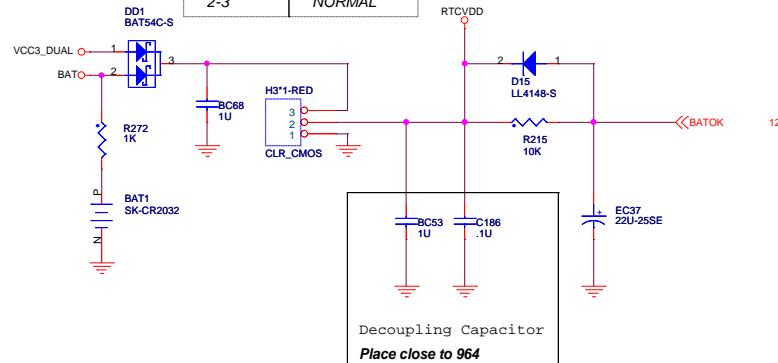


Intel Front Panel



For Acer

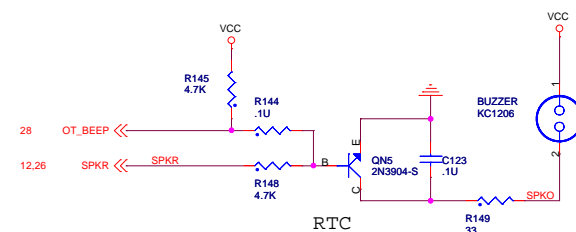
CLR_CMOS	CLEAR CMOS
1-2	CLEAR
2-3	NORMAL



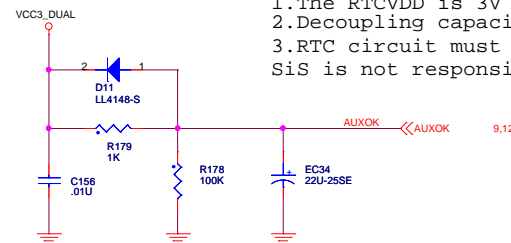
Decoupling Capacitor
Place close to 964

NOTE!

- 1.The RTCVDD is 3V
 - 2.Decoupling capacitor must be close to 635 RTCVDD pin.
 - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.



RTC



1. BOM Attention

(1) South Bridge

Option	SIS964	SIS964L
Components		
U13	964 964142	964L 964162
R241	374 374010	X
R71, R74	33 330000	X
R72, R75	49.9 499010	X
R331	330 330001	X
D23	1N4148 03-121-214890	X
SATA1, SATA2	10-020-007690	X

(3) On-Board VGA

Option	Support	No Support
Components		
U8	661FX 661141	648FX 648161
L30, L31, L32, L6, L7, L8	FB-120	X
C112, C116, C117, BC35	1U	X
C118, C119	.1U	X
MC36, MC37	10U	X
R136	130 130011	X
R134, R143	33	X
R128, R135	100	X
VGA1	10-717-015010	X
C111, C114, C115	22P	X
R22, R23, R24	75	X
R32, R39	2.2K	X
CV1~7	22P-VP 04-130-220003	X
F2	O	X

(3) LAN

Option	8100C 10/100 Mbps	8110S 1Gbps	8110SB 1Gbps	8201BL 10/100 Mbps	8201CL 10/100 Mbps
Components					
LAN1	RTL8100C 01-230-100351	RTL8110S 01-230-110350	RTL8110SB	RTL8201BL 02-148-201661	RTL8201CL 02-162-201660
R53	5.6K-1	2.49K-1	2.49K-1	5.9K-1	2K-1
R12, R14, R21, R28	X	49.9	X	X	X
C10, C18	X	0.1u	X	X	X
C52, C53, C54	X	0.01u	X	X	X
C51	0.1u	0.01u	0.01u	X	0.1u
RJ2	X	(1-2) 0 ohm	X	X	(2-3) 0 ohm
R604	X	X	X	X	0 ohm
C601	X	X	X	X	0.1u
L14/ C23	X	0 ohm/ 0.1u	0 ohm/ 0.1u	X	X
RJ7/ C19	(1-2)FB-600 /10u-08	X	(2-3)FB-600 /10u-08	X	X
L21	0 ohm	X	X	0 ohm	0 ohm
QP1	X	HA8550	HA8550	X	X
RJ1	(1-2) 0 ohm	(2-3) 0 ohm	(2-3) 0 ohm	X	X
RJ8	X	X	X	X	(2-3) 0 ohm
QP3	HPN2907A	HA8550	HA8550	X	X
RN601, RN602, RN603	X	X	X	4.7K-8P4R	4.7K-8P4R
C601	X	X	X	0.1u	0.1u
R608/ R609	X	X	X	4.7K/ 10K ohm	4.7K/ 10K ohm
R605	X	X	X	1.5K ohm	1.5K ohm
R602, R603, R607	X	X	X	22 ohm	22 ohm
SR600/ SR601/ SR602/ SR603/ SR607/ SR608	X	X	X	22 ohm-B	22 ohm-B
SR606	150 ohm-B	150 ohm-B	150 ohm-B	X	X
SR604/ SR605	15K/ 1K ohm-B	15K/ 1K ohm-B	15K/ 1K ohm-B	X	X
Y600/ R600	X	X	X	Y-25M/ 0 ohm	Y-25M/ 0 ohm
C166/ C600	4.7K ohm/ X	4.7K ohm/ X	4.7K ohm/ X	22P	22P
R190/ R191	X / 1K ohm	X / 1K ohm	X / 1K ohm	1K ohm/ X	1K ohm/ X
EEPROM1/ EEPROM3	O / X	O / X	O / X	X / O	X / O
R54/ R610	3.6K ohm/ X	3.6K ohm/ X	3.6K ohm/ X	X / 4.7K ohm	X / 4.7K ohm

2. GPIO Function

GPIO		Status	0	1	Jumper
GPIO5	* RESERVED		RESERVED	RESERVED	JP4
GPIO6	* RESERVED		RESERVED	RESERVED	JP5
GPIO7	* LAN Selection		LANPHY	PCILAN	N/A
GPIO9	USB, PS/2 S4/S5 Wake Up		Disable	Enable	N/A
GPIO10	DDR Voltage		2.54V	2.63V	N/A
GPIO11	* WHQL		No Support	Support	JPT3
GPIO13	Flash Write Protect		Un-Protect	Protect	

(1) "*" means that the function is selective and ECS may make changes at any time, without notice in this page.

(2) Jumper Setting (Header 3*1):

1: (1-2)

0: (2-3)

(3) Please see Page.12 for more detail jumper function.

JPT3		1-2	2-3
GPIO11		1	0
HP	Clear CMOS	Normal	Clear
TRIGEM	Suspen Mode	S1 & S3	S1

JPT4		1-2	2-3
GPIO5		1	0
HP	Clear Password	Normal	Clear
TRIGEM	BIOS Logo	TG	Commaeul

